A Time-Interleaved Ring-VCO with Reduced 1/f^3 Phase Noise Corner, Extended Tuning Range and Inherent Divided Output

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***Abstract*— This paper describes a time-interleaved (TI) ring-VCO (RVCO) exhibiting an improved phase noise over a wide range of frequency offsets, an extended tuning range and an inherent divided output. Such features are achieved by substantially increasing the number of delay stages in a RVCO, such that the rich multi-phase sub-outputs can be combined through a time-interleaved method, generating a high-frequency output with a significantly lowered 1/f^3 phase noise corner (f_{1/f^3}). The critical block is the phase combiner, which features a timing window to minimize the delay offset and mismatch. A reconfigurable TI factor extends the tuning range over the same range of supply voltage (V_{DD}). The prototype is a 35-stage dual-mode TI-RVCO occupying 0.003 mm^2 in 65 nm CMOS, and has a selectable TI factor of 5 and 7. The measured f_{1/f^3} is 150 kHz at 3.47 GHz, which is 6.2× less than that of a typical 5-stage RVCO. The tuning range covers 1.7 to 3.5 GHz (68.5%) over V_{DD} = 0.7 to 1 V. The multi-phase sub-outputs are the inherent divided output (÷ 5 or ÷ 7) that can be directly utilized in a PLL to save area and power.**

***Index Terms*— 1/f^3 phase noise corner, divided output, flicker noise, impulse sensitivity function (ISF), phase combiner, phase noise, ring voltage-controlled oscillator (RVCO), supply voltage, time-interleaved (TI).**

I. Introduction

With the improved device f_t and parasitic effects of ultra-scaled CMOS technologies, the tiny-area ring voltage-controlled oscillator (RVCO) [1] is rekindled as a potential replacement of the bulky LC-VCO for GHz-range radios [2]. Especially for multi-channel RF systems that have numerous inductors and frequency sources, using the RVCO can avoid the problem of magnetic pulling, and can cover a wide frequency range. Yet, at the same power budget, the RVCO has a higher phase noise than that of the LC-VCO from low to high frequency offsets. Recent efforts on the RVCO aim to break such a phase noise limit at the phase-locked loop (PLL) system level. Typically, the loop bandwidth of a type-II PLL is restricted by the Gardner's Limit of $f_{REF}/10$, to guarantee the loop stability. It is, however, far from adequate to suppress the close-in phase noise (PN) if a RVCO is used. In [3], a type-I PLL as shown in Fig. 1(a) succeeds in suppressing the PN of the RVCO by extending the loop bandwidth to $f_{REF}/2$ (~10 MHz), resulting in a 0.015 mm^2 inductorless frequency synthesizer in 45 nm CMOS satisfying the 2.4 GHz WLAN specifications.

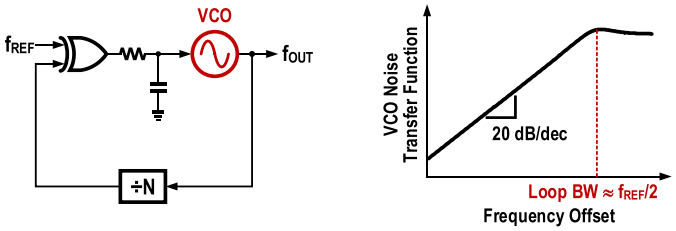

Fig. 1. (a) A typical type-I PLL and (b) its noise transfer function for the VCO. The VCO can be a RVCO [3].

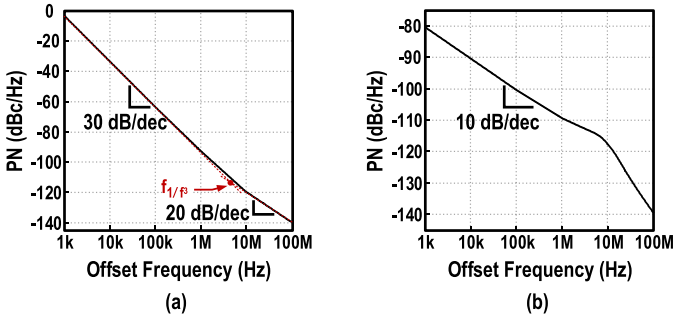

Fig. 2. (a) PN of a typical RVCO and (b) PN of a type-I PLL accounting only the PN contribution of the RVCO.

Nevertheless, the RVCO's PN suppression offered by a type-I PLL is limited to 20 dB/dec [Fig. 1(b)], which is inadequate to suppress the RVCO's PN in the 1/f^3 region, where the PN goes up 30 dB/dec in low offset frequencies [Fig. 2(a)]. As a result, the PLL's output PN due to the RVCO still has a slope of 10 dB/dec until the 1/f^3 PN corner (f_{1/f^3}) [Fig. 2(b)], degrading the overall jitter performance of the PLL. This point is evident in [3], as its f_{1/f^3} is still high (~4 MHz) even employing large transistors (W/L = 36/0.28 μm). Cascading a time-amplified clock-skew sub-sampling DLL [4] can further suppress the close-in phase noise while maintaining a large loop bandwidth, but the cascaded stages will add noise at the

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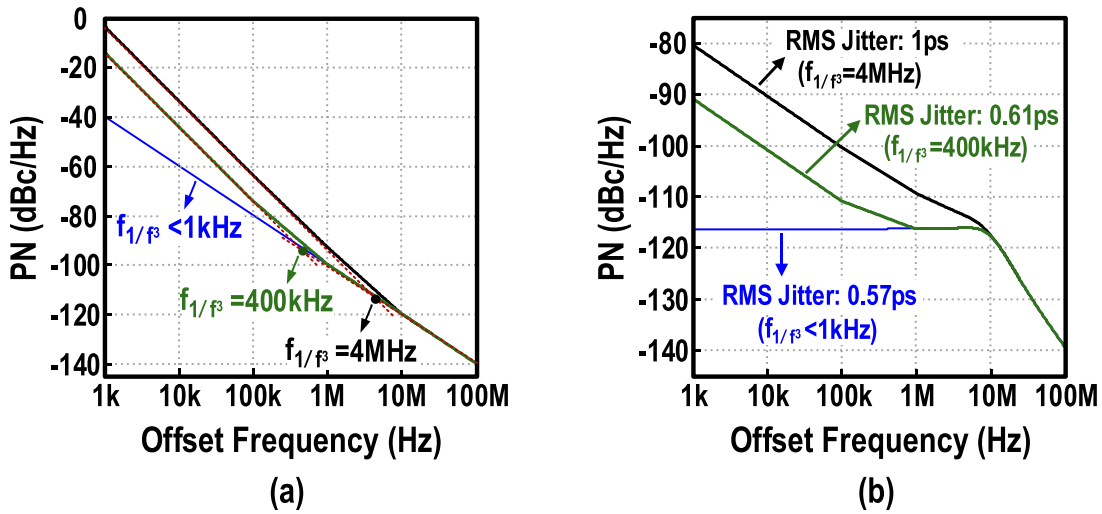

Fig. 3. PN reduction of (a) the RVCO and (b) the type-I PLL by reducing the f_{1/f^3} of the RVCO.

offset frequencies out of the loop bandwidth and increase the power consumption and chip area. The sub-sampling operation also generates a large reference spur. If it is possible to reduce the f_{1/f^3} of the RVCO by 10× from 4 to 0.4 MHz [Fig. 3(a)], the RMS jitter of the PLL would be reduced by 39% (1 to 0.61 ps), assuming a type-I PLL with a loop bandwidth of 10 MHz [Fig. 3(b)]. Thus, it is worthwhile to explore a circuit technique that can effectively reduce the f_{1/f^3} of the RVCO.

This paper describes a time-interleaved (TI) RVCO (TI-RVCO) exhibiting interesting properties. The experimental prototype [5] confirms an effective reduction of the f_{1/f^3} (∼1 MHz → ∼100 kHz), resulting in lower phase noise over a wide range of frequency offsets (10 kHz to 1 MHz) at the same power budget. Other key features are an extended tuning range by reconfiguring the TI factors, and an inherent divided output ready as the feedback frequency in the PLL to save power and area.

Section II analyzes the f_{1/f^3} of the RVCO based on the time-variant PN model. The concept of the proposed TI-RVCO is described in Section III, and its circuit implementation is detailed in Section IV. Section V discusses the experimental results, and the conclusions are drawn in Section VI.

II. 1/f³ PN Corner of RVCO

According to the time-variant phase noise model [6], the f_{1/f^3} of a CMOS VCO comes from the upconversion of the transistor's flicker noise, which can be predicted by the impulse sensitivity function (ISF). Generally, the PN of the RVCO at an offset frequency Δf from its fundamental frequency can be expressed as [7]:

$$\mathcal{L}(\Delta f) = 10\log_{10}\left[\frac{\sum_i N_{L,i}}{8\pi^2 q_{max}^2 (\Delta f)^2}\right] \quad (1)$$

where q_{max} is the maximum charge displacement across the capacitor at each output node, and $N_{L,i}$ is the effective current noise power produced by i^{th} MOS device given by:

$$N_{L,i} = \frac{1}{2\pi}\int_0^{2\pi} \Gamma_i^2(\phi)\,\overline{i_{n,i}^2(\phi)}\,d\phi \quad (2)$$

where $\overline{i_{n,i}^2(\phi)}$ is the thermal noise power density of the i^{th} noise source, and Γ_i is the ISF function that characterizes the current noise to phase conversion properties of the corresponding noise source. Differing from the LC-VCO, in the RVCO the noise power $\overline{i_{n,i}^2(\phi)}$ reaches its maximum during the edge transition when Γ_i is also at maximum. Thus, the cyclostationarity of the current noise can be ignored by representing $\overline{i_{n,i}^2(\phi)}$ with its maximum $\overline{i_{n,max,i}^2}$ [6].

Then, the $1/f^2$ PN due to the thermal noise of the MOS device is given by:

$$N_{L,i} = \Gamma_{rms,i}^2\,\overline{i_{n,max,i}^2} \quad (3)$$

where $\Gamma_{rms,i}$ is the rms value of the ISF Γ_i. Since the noise currents injected by the NMOS and PMOS devices in a typical N-stage inverter-based RVCO (N is an odd number) can be regarded as uncorrelated [8], their effective current noise powers can be superposed. Thus the phase noise in $1/f^2$ region can be obtained using (1) by summing the 2N noise sources from NMOS and PMOS:

$$\mathcal{L}_{1/f^2}(\Delta f) = 10\log_{10}\left[\frac{N(1+\beta A_1)\,\Gamma_{rms,PMOS}^2\,\overline{i_{n,max,PMOS}^2}}{8\pi^2 q_{max}^2 (\Delta f)^2}\right] \quad (4)$$

where $\beta = \overline{i_{n,max,NMOS}^2}/\overline{i_{n,max,PMOS}^2}$, $A_1 = \Gamma_{rms,NMOS}^2/\Gamma_{rms,PMOS}^2 = \lambda^3$, and the subscript i in (1) –(3) is substituted by NMOS or PMOS in (4). Replacing $\Gamma_{rms,PMOS}^2$ in (4) with (21) given in the Appendix, the relationship between the $1/f^2$ phase noise and the number of stages N can be obtained as:

$$\mathcal{L}_{1/f^2}(\Delta f) = 10\log_{10}\left[\frac{1}{N^2}\cdot\frac{1}{3q_{max}^2(\Delta f)^2}\cdot\frac{(1+\beta\lambda^3)}{\eta^3(1+\lambda)^3}\cdot\overline{i_{n,max,PMOS}^2}\right] \quad (5)$$

Since the $1/f^3$ phase noise only comes from the frequency upconversion of the low frequency noise, the corresponding

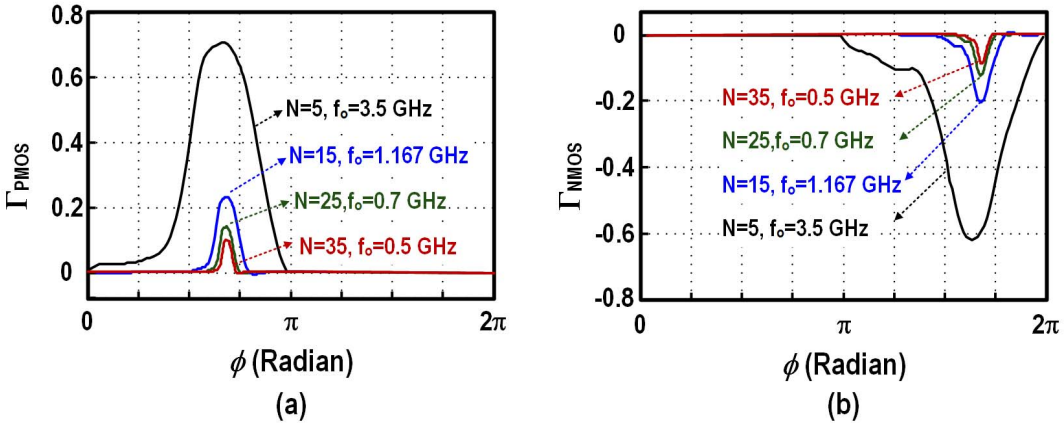

Fig. 4. Simulated ISFs for the PMOS and NMOS devices in the RVCOs with different numbers of delay stages (V_{DD} = 1 V): (a) Γ_{PMOS} and (b) Γ_{NMOS}.

$N_{L,i}$ is different from that for the $1/f^2$ noise as given by [6]:

$$N_{L,i} = \Gamma_{DC,i}^2 \overline{i_{n,max,1/f,i}^2} \tag{6}$$

where $\Gamma_{DC,i}$ is the DC value of the ISF Γ_i, and $\overline{i_{n,max,1/f,i}^2}$ is the maximum 1/f noise current of the i^{th} noise source during one cycle. The power density of 1/f and thermal noise current can be related using the 1/f noise corner $f_{1/f}$ as:

$$\overline{i_{n,max,1/f,i}^2} = \overline{i_{n,max,i}^2} \cdot \frac{f_{1/f,i}}{\Delta f} \tag{7}$$

Here the offset frequency Δf is used since $\overline{i_{n,max,1/f,i}^2}$ represents the flicker noise power density after frequency upconversion. By putting (6) and (7) into (1) and summing the 2N noise sources from NMOS and PMOS, the phase noise in $1/f^3$ region can be obtained as:

$$\mathcal{L}_{1/f^3}(\Delta f) = 10\log_{10}\left[\frac{N(1+\alpha\beta A_2)\Gamma_{DC,PMOS}^2 \overline{i_{n,max,PMOS}^2}}{8\pi^2 q_{max}^2 (\Delta f)^3} \cdot f_{1/f,PMOS}\right] \tag{8}$$

where $A_2 = \Gamma_{DC,NMOS}^2/\Gamma_{DC,PMOS}^2$, $\alpha = f_{1/f,NMOS}/f_{1/f,PMOS}$, and the subscript i in (1) – (3), (6), and (7) is substituted by NMOS or PMOS in (8). Replacing $\Gamma_{DC,PMOS}^2$ in (8) with (22) from the Appendix, the relationship between the $1/f^3$ phase noise and N can be obtained as:

$$\mathcal{L}_{1/f^3}(\Delta f) = 10\log_{10}\left[\frac{1}{N^3} \cdot \frac{1}{2q_{max}^2(\Delta f)^3} \cdot \frac{(1+\alpha\beta\lambda^4)}{\eta^4(1+\lambda)^4} \cdot \overline{i_{n,max,PMOS}^2} \cdot f_{1/f,PMOS}\right] \tag{9}$$

According to (5) and (9), the $1/f^2$ phase noise is proportional to $1/N^2$, while the $1/f^3$ phase noise is proportional to $1/N^3$. Thus the $1/f^3$ phase noise decreases faster than the $1/f^2$ phase noise when N increases, which indicates the f_{1/f^3} will be reduced.

By equating the $1/f^2$ phase noise from (4) and $1/f^3$ phase noise from (8), the relationship between f_{1/f^3} and $f_{1/f}$ of NMOS and PMOS devices can be obtained as:

$$f_{1/f^3} = f_{1/f,PMOS} \cdot \frac{\Gamma_{DC,PMOS}^2}{\Gamma_{rms,PMOS}^2} \cdot \frac{1+\alpha\beta A_2}{1+\beta A_1} \tag{10}$$

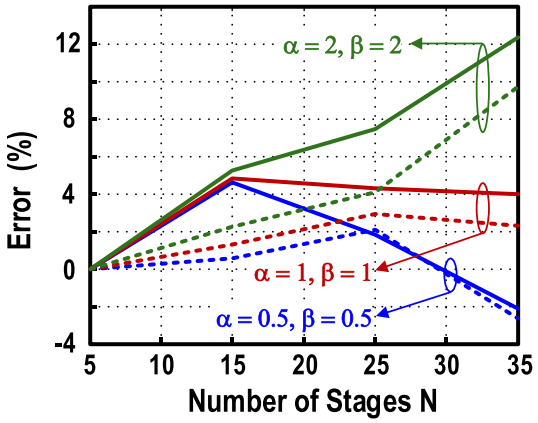

Fig. 5. Difference between the calculated and simulated normalized f_{1/f^3} (solid line for V_{DD} = 1 V and dash line for V_{DD} = 0.7 V).

Again, replacing $\Gamma_{rms,PMOS}^2$ and $\Gamma_{DC,PMOS}^2$ with (21) and (22) from the Appendix, (10) can be rewritten as:

$$f_{1/f^3} = f_{1/f,PMOS} \cdot \frac{3}{2\eta} \cdot \frac{1}{N} \cdot \frac{1+\alpha\beta\lambda^4}{(1+\beta\lambda^3)(1+\lambda)} \tag{11}$$

Given the transistor sizes and supply voltage (V_{DD}), $f_{1/f,PMOS}$, α, β and λ will keep unchanged, and thus the f_{1/f^3} is $\propto$ 1/N. If N increases from N_1 to N_2, the f_{1/f^3} will be reduced by a ratio of N_2/N_1. According to (11), this relationship between f_{1/f^3} and N does not require that the 1/f noise corner of NMOS and PMOS devices are identical ($\alpha = 1$), and the normalized rising and falling edges are symmetrical ($\lambda = 1$). Further, the equation in [5] is a simplified expression of (11) when $\alpha = \lambda = 1$.

Fig. 4 shows the simulated Γ_{NMOS} and Γ_{PMOS} for the RVCOs with different numbers of delay stages. All delay stages are CMOS inverters featuring the same size (W/L = 14/0.18 μm for PMOS, and W/L = 7/0.18 μm for NMOS). The simulated Γ_{NMOS} and Γ_{PMOS} are then employed to obtain the simulated f_{1/f^3} according to (10). To avoid the effect caused by the unknown parameter η in (11), the normalized f_{1/f^3} (defined as the ratio between the f_{1/f^3} for the RVCOs with different numbers of stages and the f_{1/f^3} for the 5-stage RVCO) is used to compare (11) with the simulation results. As plotted in Fig. 5, the errors between the calculated

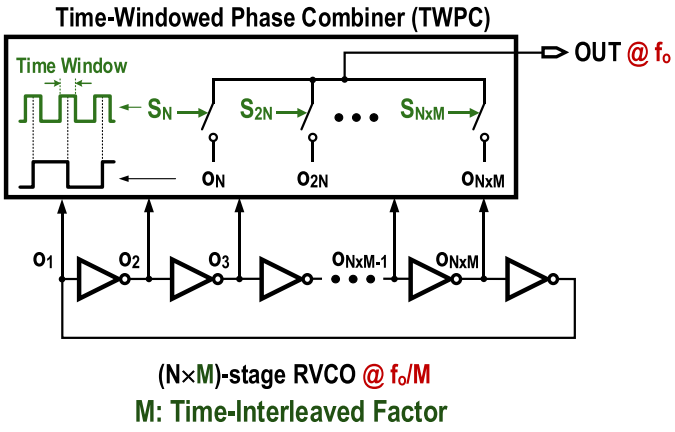

Fig. 6. Simplified schematic of the proposed TI-RVCO.

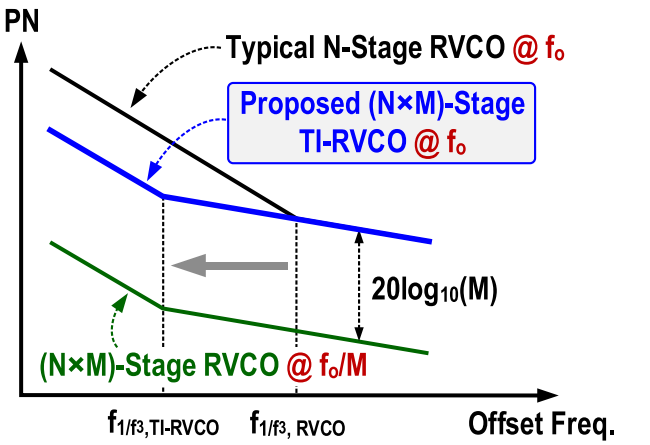

Fig. 7. PN profiles of the N-stage RVCO, (N × M)-stage RVCO and proposed (N × M)-stage TI-RVCO.

and simulated normalized f_{1/f^3}, for different combinations of α, β at $V_{DD} = 1$ V and 0.7 V are within +13%/4% as given by:

$$\text{Error} = \frac{\text{Calculated normalized } f_{1/f^3} - \text{Simulated normalized } f_{1/f^3}}{\text{Simulated normalized } f_{1/f^3}} \tag{12}$$

Since the calculated normalized f_{1/f^3} obtained from (11) does not depend on α, β and V_{DD}, the simulation results indicate the normalized f_{1/f^3} is a weak function of these three variables.

Still, reducing the f_{1/f^3} by simply increasing the number of delay stages while keeping the same transistor size and V_{DD} would inevitably decrease the oscillation frequency. Thus, this paper introduces a TI-RVCO that can recover a high frequency output from the rich multi-phase sub-outputs generated by a large number of delay stages, as presented next.

III. Principles of the TI-RVCO

Fig. 6 shows the simplified schematic of the proposed TI-RVCO. To reduce the f_{1/f^3} of a typical N-stage RVCO operating at f_o, the number of stages is increased from N to N × M (M is also an odd number). According to (11), the f_{1/f^3} of the (N × M)-stage RVCO would be reduced by M times when compared with that of the original N-stage RVCO. Although the operating frequency of the (N × M)-stage RVCO drops to f_o/M, it contains a large number of sub-outputs with different phases, which can be properly combined through a time-windowed phase combiner (TWPC) sharing a similar concept as the phase-rotating technique used in the fractional divider [9] to recover a high frequency output at f_o.

A. PN Performance

As long as the time windows are non-overlapping and long enough to fully house the rising and falling edge of the selected sub-outputs, the additional noise contribution from the TWPC would be negligibly small. Thus the RMS jitter of the combined output signal will remain the same as that of a (N × M)-stage RVCO, while the output frequency is increased by a factor M. On the other hand, the RMS jitter is obtained by integrating the phase noise [10]:

$$J_{RMS}^2 = 2 \cdot \left(\frac{1}{2\pi f}\right)^2 \cdot \int_0^{\infty} 10^{\frac{\mathcal{L}(\Delta\omega)}{10}} d(\Delta\omega) \tag{13}$$

Thus the phase noise of the combined output at f = f_o is increased by $20\log_{10}(M)$ [dB] compared with that of the output of a (N × M)-stage RVCO operating at f_o/M. Thus, the PN profile of an (N × M)-stage TI-RVCO is just an M^2-time-upshifted version of a typical (N × M)-stage RVCO as shown in Fig. 7, while keeping the f_{1/f^3} unchanged. As a result, the (N × M)-stage TI-RVCO reduces the f_{1/f^3} by M times while still maintaining the same output frequency at f_o when compared with a typical N-stage RVCO using the same delay stage.

The TI technique will not degrade the $1/f^2$ phase noise at large frequency offset which is induced by the transistor's thermal noise. According to (5), the $1/f^2$ phase noises of a N-stage and a (N × M)-stage RVCO are proportional to $1/N^2$ and $1/(N \times M)^2$, respectively. Since the $1/f^2$ phase noise of the (N × M)-stage TI-RVCO output at f_o is M^2 times to that of the (N × M)-stage RVCO, it is also proportional to $1/N^2$ and equals to that of the N-stage RVCO operating at f_o.

B. Choice of the TI Factor

For a (N × M)-stage TI-RVCO, M is defined as the TI factor, which decides many important properties of the TI-RVCO. Enlarging M can further reduce f_{1/f^3}, but extra phases will be required for combination to recover the same f_o, which would exacerbate the delay mismatches in the TWPC and subsequently adding difficulty to the layout, thus raising the output spur level. Since the output spurs due to the phase mismatch appear at the vicinity of f_o, i.e., $\pm h \times (f_o/M)$ where $h = 1, 2, 3, \ldots, M-1$, a large M will also move the output spurs closer to the fundamental frequency f_o. On the other hand, from the PLL's viewpoint, the $1/f^3$ noise of the RVCO at a small frequency offset lower than several hundreds of kHz is less critical, since its absolute value is quite small after integrating within a small frequency range and the contribution

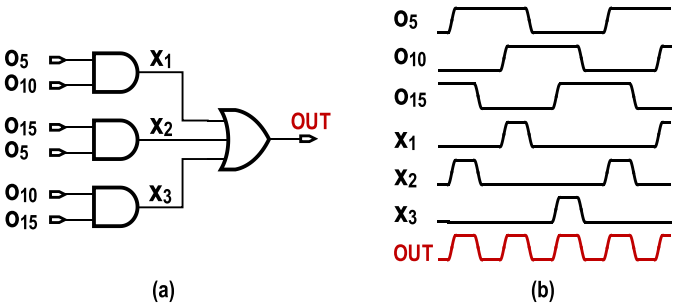

Fig. 8. (a) Schematic and (b) timing diagram of the conventional phase combiner [11].

to the overall RMS jitter is ignorable. For instance, when the f_{1/f^3} of the RVCO in Fig. 3(a) is further reduced from 400 kHz to lower than 1 kHz, the PLL output RMS jitter is only reduced by 0.04 ps from 0.61 to 0.57 ps as shown in Fig. 3(b). Thus, as the typical f_{1/f^3} of a RVCO is around several MHz in advanced CMOS technologies, a practical value of M can be 5 or 7, which is adequate to reduce the f_{1/f^3} to several hundreds of kHz without compromising much the spur level, power consumption and die area.

C. Uniqueness of the Oscillation Frequency

Theoretically, it seems possible for a (N × M)-stage RVCO (with and without TI) to oscillate at other higher frequencies $N\times(f_o/M)$ and f_o, when the phase shift of the loop equals to $N\times(2\pi)$ and $M\times(2\pi)$, respectively. However, because the mismatch among the delay stages will eventually force the oscillation frequency back to f_o/M, the (N × M)-stage RVCO can only oscillate at the lowest frequency in the steady state, i.e., f_o/M, when the phase shift of the loop equals to 2π.

For example, in a 35-stage RVCO (N = 5), if the initial voltages of o_i (i = 5, 10, 15, 20, 25, 30, 35) are forced to the same voltage level (e.g., 0 V) in the simulation, the RVCO will oscillate at the same frequency f_o as the 5-stage RVCO when starting up and the voltage waveforms of o_i (i = 5, 10, 15, 20, 25, 30, 35) are all in phase. However, if the loading capacitance of node o_i (i = 1, 2, 3, 4, 5) is slightly smaller (e.g., 0.1 fF) than that of the other nodes, the oscillation frequency of the RVCO will be forced back to $f_o/7$ within 30 ns. A similar phenomena is observed when forcing the initial voltages of o_i (i = 7, 14, 21, 28, 35) to 0 V in the simulation. The RVCO will oscillate at the frequency $5f_o/7$ first, and then return to the stable frequency $f_o/7$ in 470 ns, if the loading capacitances of node o_i (i = 1, 2, 3, 4, 5, 6, 7) is 0.1 fF smaller than that of the other nodes.

IV. Implementation of a Dual-Mode TI-RVCO

A. Time-Windowed Phase Combiner (TWPC)

The phase combiner is a critical block in the TI-RVCO. It should be power efficient, and add minimum delay offset and mismatch between the different phases which, otherwise, would cause deterministic jitter or output spurs. Here, the delay offset is defined as the difference between the maximum/minimum value and the average value of the delays from the selected phases to the output. Fig. 8 shows the

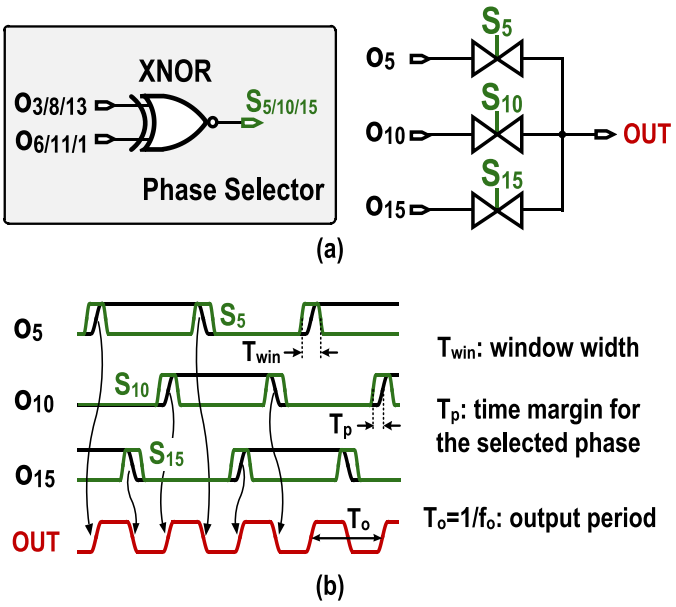

Fig. 9. (a) Schematic and (b) timing diagram of the proposed TWPC.

conventional phase combiner commonly used in the DLL-based clock multiplier [11], which suffers from a severe delay offset due to the asymmetrical inputs of the OR gate. In this work, a time-windowed phase combiner (TWPC) as shown in Fig. 9(a) is proposed to eliminate the delay offset. Since each selected phase can only pass through the transmission gate within the non-overlapping time window ($S_{5,10,15}$), the delay of each path can be well matched. Each non-overlapping time window as shown in Fig. 9(b) is created using the two adjacent phases (before and after the selected phase). To ensure all time windows in a (N×M)-stage TI-RVCO are non-overlap, the window width T_{win} is upper-bounded by

$$T_{win} \le T_o \times \frac{N-2}{2N} \tag{14}$$

where $T_o = 1/f_o$ and $N \ge 5$. Thus, logics in the phase selector are uncritical and can be minimally sized to save power since T_{win} is long enough to tolerate reasonable PVT variations and mismatches. From Monte Carlo (MC) simulations at $f_o = 3.5$ GHz (N = 5, M = 3) and at the room temperature of 27 C, the T_{win} is 92.3 ps (σ = 1.2 ps) and the time margin for the selected phase T_p is 29.7 ps (σ = 0.77 ps) for the rising edge, while the T_{win} is 87.2 ps (σ = 1 ps) and the T_p is 33.2 ps (σ = 0.69 ps) for the falling edge, ensuring both the rising and falling edge of each phase is captured within T_{win}. Table I compares the simulated delay offset and delay mismatch under the typical corner between the conventional phase combiner and the TWPC. It is clear that the proposed TWPC achieves a negligible delay offset, while reducing the delay mismatch by 3.4× (for rising edge) and 5× (for the falling edge) under the same power budget of 0.1 mW at an output frequency of 3.5 GHz.

B. Dual-Mode TI Configuration

In order to maintain a constant RMS jitter performance at the PLL output, it is preferable to decrease the phase noise of the RVCO with frequency, keeping the normalized

TABLE I

SIMULATED OUTPUT PERIOD MISMATCH OF THE 35-STAGE DUAL-MODE TI-RVCO DUE TO THE DEVICE MISMATCH IN DELAY STAGES (×7 MODE, MC SIMULATIONS WITH 500 RUNS, T = 27 °C)

	Rising Edge		Falling Edge	
	Delay Offset (ps)	Delay Mismatch (ps)	Delay Offset (ps)	Delay Mismatch (ps)
Conventional (Fig. 8)	+2 / −1.5	0.41	+3 / −3.5	0.55
Proposed (Fig. 9)	+0.005 / −0.001	0.12	+0.005 / −0.002	0.11

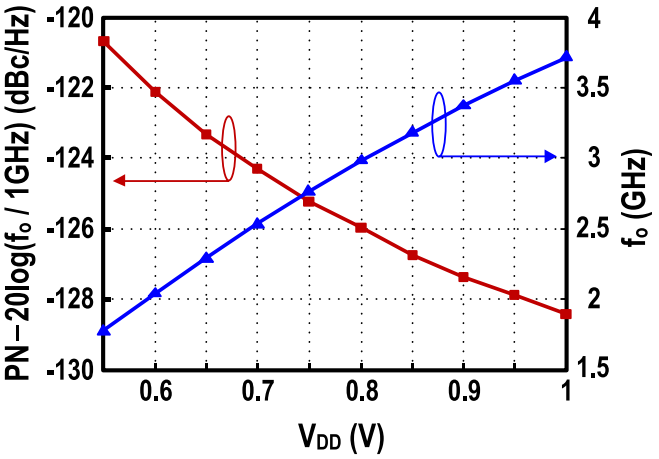

Fig. 10. Simulated normalized phase noise with frequency at 10MHz offset frequency and oscillation frequency of a 5-stage ring VCO versus V_{DD}.

phase noise [i.e., $PN - 20\log(f_0/1\ GHz)$] constant with carrier frequency f_0. Yet, a typical RVCO using a V_{DD}-based frequency tuning scheme can suffer from a degraded normalized phase noise performance at a low V_{DD} due to the increase of the effective current noise power and the decrease of the output swing. As suggested by simulation (Fig. 10), when V_{DD} decreases from 1 to 0.55 V, a frequency tuning range from 1.7 to 3.7 GHz (74%) can be covered, but the normalized phase noise at 1.7 GHz is degraded by 7.8 dB when compared with that at 3.7 GHz. If the frequency tuning range can be reduced by half only from 2.5 GHz to 3.7 GHz (39%), the required V_{DD} range can be narrowed (1 to 0.7 V), and the normalized phase noise degradation at 2.5 GHz will be reduced to 4.1 dB.

In the proposed TI-RVCO, the tuning range is extended by reconfiguring the TI factor M. As shown in Fig. 11(a), assuming N × M can be factored as the product of two odd numbers p and q (p < q), then the combined frequency can be tuned to two different bands by choosing N = p, M = q (×q mode) or N = q, M = p (×p mode). In each frequency band, the normalized PN with frequency are kept in the same range as shown in Fig. 11(b), which prevents the degradation of the normalized PN at low band. Usually a continuous tuning range is favored which requires an overlap between the two frequency bands. Thus, the condition $p \times f_2 > q \times f_1$ must be met, which indicates that the original tuning range TR_0 of the (N × M)-stage RVCO must satisfy the following conditions:

$$TR_0 = \frac{2(f_2 - f_1)}{(f_2 + f_1)} > \frac{2(q - p)}{q + p} \tag{15}$$

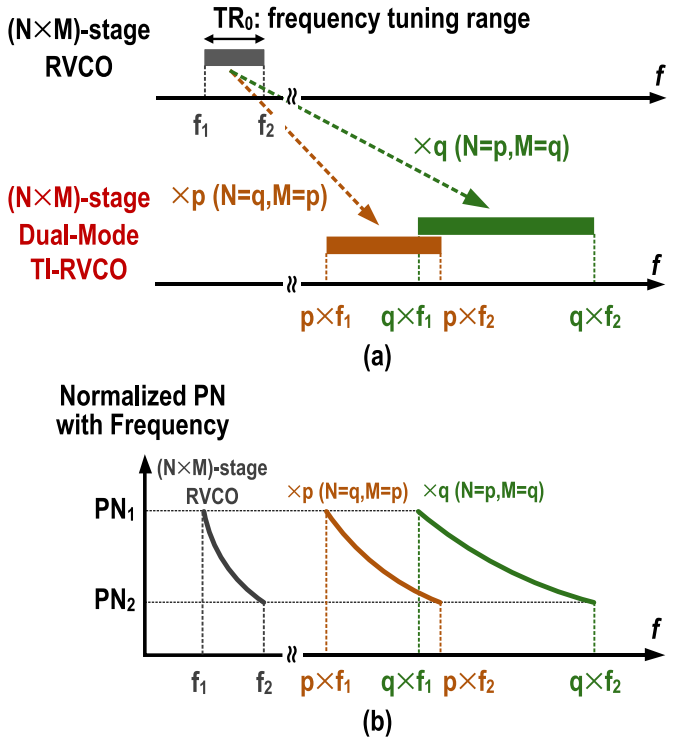

Fig. 11. (a) Frequency plan of the dual-mode TI-RVCO to ensure overlapping and (b) normalized PN with frequency in each mode.

By selecting p = 5 and q = 7 in a 35-stage TI-RVCO, the TR_0 of 39% is enough to guarantee the frequency overlap between the two output frequency bands, resulting in a roughly doubled output frequency range of 69%. Also, as discussed in Section III, the choice of M equal to 5 or 7 is large enough to reduce the f_{1/f^3} from 1 MHz to ≤ 200 kHz.

Fig. 12 shows the schematic of the proposed 35-stage dual-mode TI-RVCO, where the inverter (INV) is used as the delay stage and two separate TWPCs are utilized to select different phases in the two modes. The phases used in each mode come from two sets of inverter buffers (INV_a and INV_b) to balance the loading of each delay stage. In ×5 mode, five phases (a_1, a_8, a_{15}, a_{22}, a_{29}) are combined to generate OUT_L at 5 times of the frequency of the 35-stage RVCO. In ×7 mode, seven phases (b_1, b_6, b_{11}, b_{26}, b_{21}, b_{26}, b_{31}) are combined to generate OUT_H at 7 times of the frequency of the 35-stage RVCO. In each mode, the window width T_{win} is maximized ($5T_o/14$ for ×5 mode and $3T_o/10$ for ×7 mode) according to (14). Finally, OUT_L and OUT_H can be combined through a MUX to generate a single-phase output.

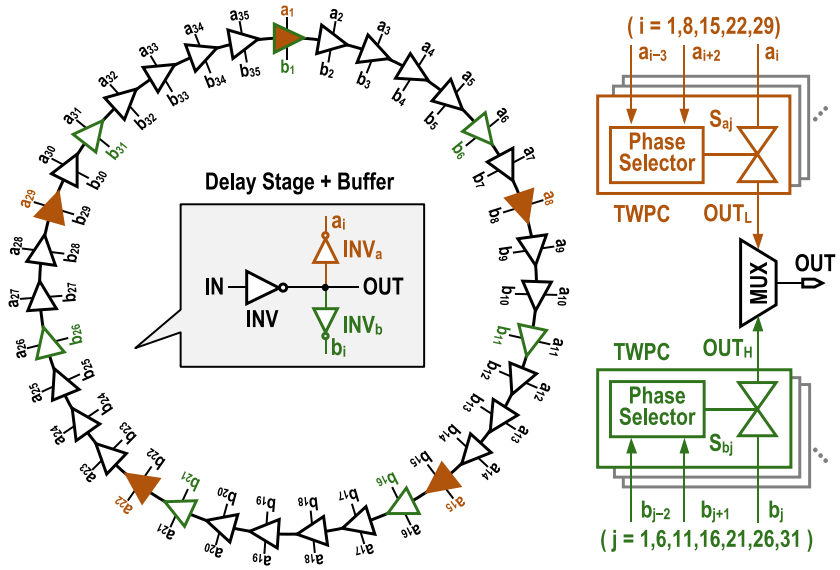

Fig. 12. Schematic of the proposed 35-stage dual-mode TI-RVCO.

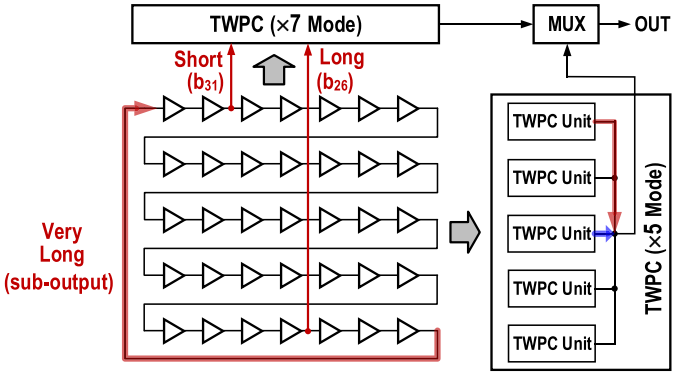

Fig. 13. Layout floor plan of the proposed 35-stage dual-mode TI-RVCO.

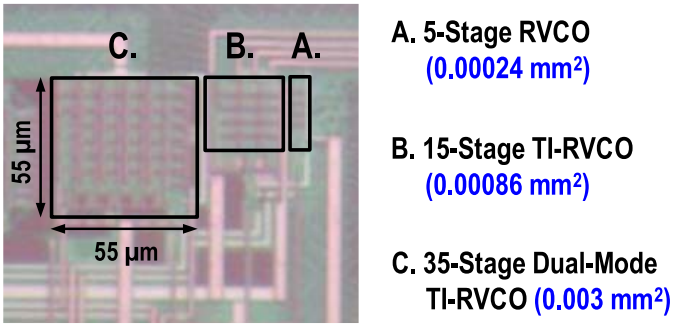

Fig. 14. Chip photo of the typical 5-stage RVCO (A), 15-stage TI-RVCO (B) and 35-stage dual-mode TI-RVCO (C).

C. Floorplan and Mismatch-Induced Spur

Fig. 13 shows the layout floor plan for the 35-stage dual-mode TI-RVCO. The output spurs induced by phase mismatch emerge mainly from the following two sources:

(i) Random mismatch between the MOS devices in the delay stages will induce a mismatch between the selected phases. To obtain good matching between these MOS devices, all the devices are put in the same orientation and the numbers of column and row are kept close to achieve a square area in the layout. According to the MC simulation results given in Table II in ×7 mode, the σ of the output period mismatch $\Delta T_o$is smaller than 0.8 ps when the average period $T_o = 281.3$ ps. Assuming that within every 7 output cycles, one cycle has a period of $T_o + \Delta T_o$ and the other 6 cycles have the same period of $T_o - (\Delta T_o/6)$, then the average period is still kept to T_o. Thus, the output spur located at $f_o \pm f_o/7$ can be estimated by $20\log_{10}(\Delta T_o/T_o)$ [12]. By choosing $\Delta T_o = \sigma$ or 3σ, it can be determined that the typical spur level is < -50 dBc while the worst spur level is around 41 dBc.

(ii) Deterministic mismatch due to the asymmetry of the layout also induces mismatch between the selected phases. As shown in Fig. 13, the different wire lengths when connecting the delay stages, the connections from the RVCO's outputs to the TWPC, and the connections at the outputs of TWPC units, will all introduce mismatches between the selected phases. These deterministic mismatches can likely be reduced by the layout effort as well as the delay compensation in each TWPC unit since they can be well predicted by post-layout simulations.

V. Experimental Results

Three prototypes were fabricated in 65 nm CMOS (Fig. 14) for comparison: a 35-stage dual-mode TI-RVCO (0.003 mm^2), a 15-stage TI-RVCO (0.00086 mm^2) and a typical 5-stage RVCO (0.00024 mm^2). All delay stages in the three prototypes use the same CMOS inverters (W/L = 14/0.18 μm for PMOS, and W/L = 7/0.18 μm for NMOS).

The phase noises at offset frequencies from 4 kHz to 40 MHz measured by Keysight E5052B Signal Source Analyzer are shown in Fig. 15. At $V_{DD} = 1$ V [Fig. 15(a)], the f_{1/f^3} of the 35-stage dual-mode TI-RVCO is reduced by 6.2× (930 → 150 kHz) when compared with that of a typical 5-stage RVCO, which follows closely the prediction by the ISF theory (7×). The output frequency of the dual-mode TI-RVCO is lower (by 280 MHz) due to the extra buffers at the output of each delay stage when compared with that of the 5-stage

TABLE II

SIMULATED OUTPUT PERIOD MISMATCH OF THE 35-STAGE DUAL-MODE TI-RVCO DUE TO THE RANDOM MISMATCH (×7 MODE, MC SIMULATIONS WITH 500 RUNS, T = 27 °C)

i^{th} No. of period	1st	2nd	3rd	4th	5th	6th	7th
Mean of T_o (ps)	281.3	281.3	281.1	281.5	281.3	281.2	281.4
σ of T_o (ps)	0.72	0.7	0.71	0.77	0.72	0.72	0.73

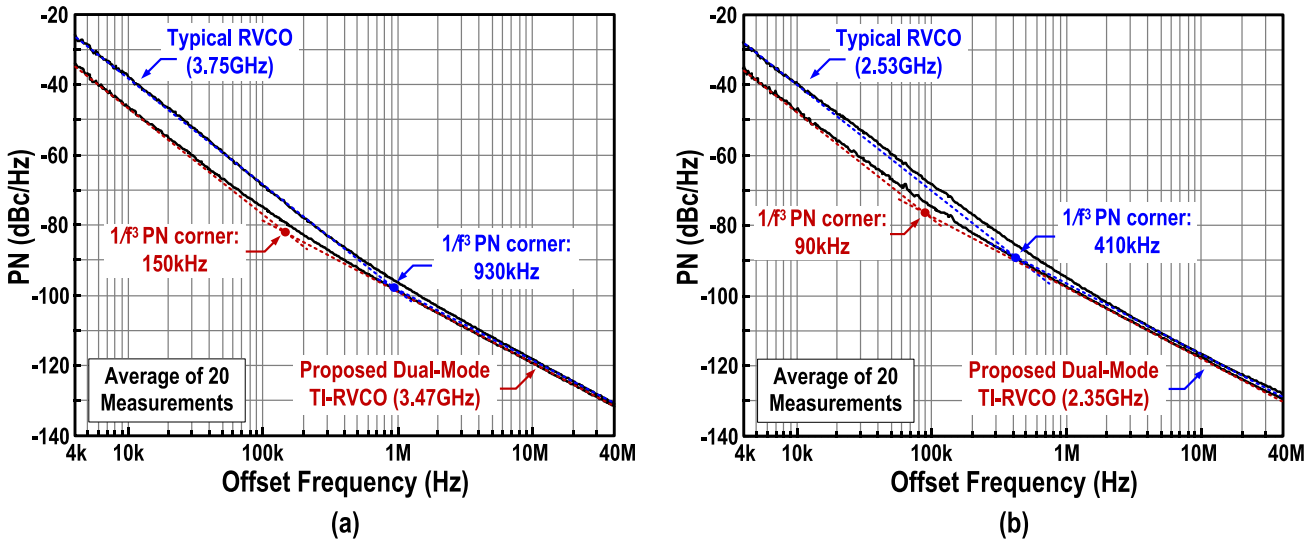

Fig. 15. Measured PN of the 35-stage dual-mode TI-RVCO and typical 5-stage RVCO at (a) $V_{DD} = 1V$ and (b) $V_{DD} = 0.7V$.

RVCO. At $V_{DD} = 0.7$ V [Fig. 15(b)], the f_{1/f^3} of the 35-stage dual-mode TI-RVCO is reduced by 4.5× (410 → 90 kHz). The reason why the f_{1/f^3} improvement at lower V_{DD} becomes smaller is due to the limitation of the measurement accuracy at a low frequency offset, thus the extraction of f_{1/f^3} becomes less accurate. For an accurate extraction of the f_{1/f^3} lower than 100 kHz, the accurate phase noise measurement at frequency offset down to much lower than 4 kHz is required, which is beyond the capability of the equipment. According to the simulation results in Fig. 5, we believe that the actual improvement of the f_{1/f^3} at $V_{DD} = 0.7$ V should be close to that at $V_{DD} = 1$ V. When comparing the f_{1/f^3} of the same RVCO or TI-RVCO at different V_{DD}, it can be seen that the f_{1/f^3} is reduced at low V_{DD}, which is mainly due to the reduction of the device's intrinsic $f_{1/f}$. According to (7), the $f_{1/f}$ of a MOS device in the saturation region can be given as:

$$f_{1/f} = \overline{i_{n,1/f}^2} \cdot \frac{\Delta f}{\overline{i_n^2}} = \overline{V_{ng}^2} \cdot \frac{g_m \Delta f}{4kT\gamma} \tag{16}$$

where $\overline{V_{ng}^2}$ is the input-referred 1/f noise power density of the MOS device, γ is the excess noise factor for the device thermal noise. Thus, reducing V_{DD} will reduce g_m and thus $f_{1/f}$. In fact, $\overline{V_{ng}^2}$ will also decrease as the gate bias voltage goes down [13], which makes the reduction of $f_{1/f}$ with the decrement of V_{DD} more significant.

Fig. 16 shows the measured f_{1/f^3} for the three implementations at different V_{DD}. It can be seen that at certain V_{DD}, the f_{1/f^3} for both ×5 and ×7 modes of the 35-stage TI-RVCO are quite close, which confirms that the f_{1/f^3} does not change with the TI factor. Also, the measured f_{1/f^3} of the 35-stage dual-mode TI-RVCO is between 90 and 150 kHz, which is comparable to the state-of-the-art LC-VCOs [14] (120 to 240 kHz) and [15] (60 to 100 kHz) that already feature $1/f^3$-noise-reduction techniques.[1]

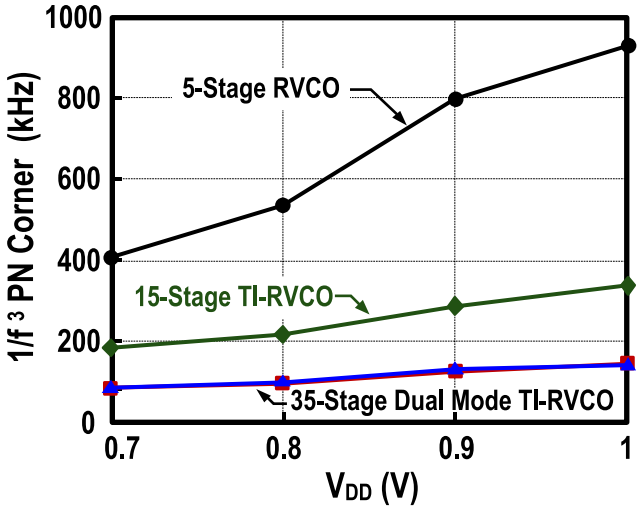

Fig. 16. Measured f_{1/f^3} of the 5-stage RVCO (circle), 15-stage TI-RVCO (diamond) and 35-stage dual-mode TI-RVCO (×5 mode: triangle; ×7 mode: square) versus V_{DD}.

[1]The low f_{1/f^3} only indicates that the $1/f^3$ phase noise is relatively small when compared with the $1/f^2$ phase noise. The absolute phase noises in the $1/f^3$ and $1/f^2$ regions of the proposed TI-RVCO are still much higher than those of the LC-VCO.

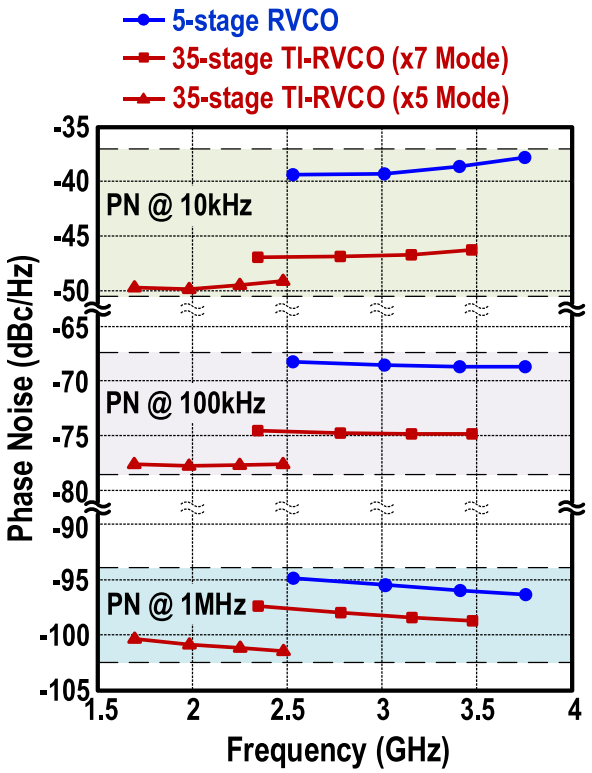

Fig. 17. Measured PN at 10 kHz, 100 kHz and 1 MHz offset frequencies of the 35-stage dual-mode TI-RVCO (×5 mode: triangle; ×7 mode: square) and 5-stage RVCO (circle) versus the carrier frequency.

To fairly compare the performance of the oscillators operating at different frequencies with different power consumption, the figure-of-merit (FoM) can be used [16]:

$$\text{FoM} = -\text{PN} + 20\log_{10}\left(\frac{f_0}{\Delta f}\right) - 10\log_{10}\left(\frac{P_{DC}}{1\text{mW}}\right) \quad (17)$$

where PN is the phase noise at a frequency offset Δf from the carrier frequency f_0 and P_{DC} is the oscillator power consumption. Fig. 17 and Fig. 18 compares the phase noise and FoM between the 35-stage dual-mode TI-RVCO and the 5-stage RVCO. The former achieves better results from 10 kHz to 1 MHz offsets, and shows a 68.5% tuning range using only 30% of V_{DD} downscaling (1 V to 0.7 V). There is adequate overlap (130 MHz) between the two frequency bands.

As shown in Fig. 19, the power consumption of the 35-stage dual-mode TI-RVCO is $\sim$ 0.5 mW/GHz at 3 GHz which is $\sim$1.5× of the 5-stage RVCO. Fig. 20 shows the measured V_{DD}-to-frequency sensitivity. The results of the 35-stage dual-mode TI-RVCO are 3.75 GHz/V for ×7 mode, and 2.62 GHz/V for ×5 mode. The former is close to that of the 5-stage RVCO (4.07 GHz/V) at a similar frequency. Thus, the TI technique should not degrade the V_{DD}-to-frequency sensitivity. Fig. 21 shows a possible architecture of the TI-RVCO based type-I PLL, the type-I loop controls small varactors (not implemented in this work) for fine frequency tuning while an auxiliary frequency locking loop for coarse frequency tuning can be employed to tune the virtual-supply node V_{reg} of the TI-RVCO through a low-dropout regulator (LDO) [17]. This dual-loop architecture allows the use of a small bandwidth of the LDO, which can reduce the susceptibility of the TI-RVCO to the V_{DD} noise without affect the bandwidth of the type-I loop.

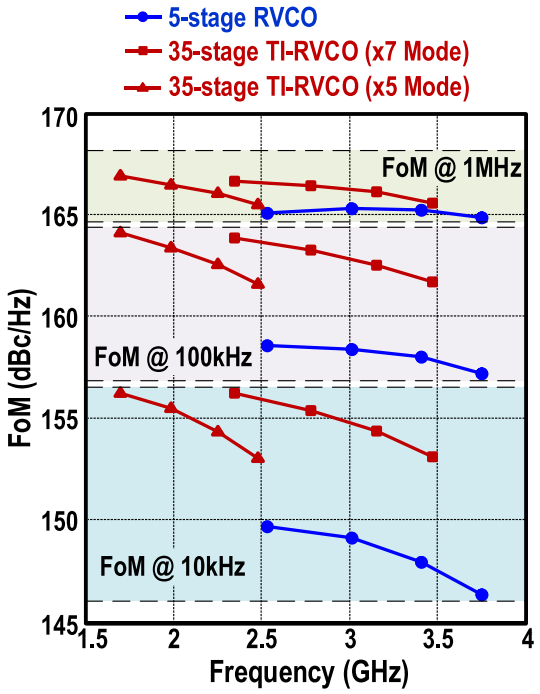

Fig. 18. Measured FoM at 10 kHz, 100 kHz and 1 MHz offset frequencies of the 35-stage dual-mode TI-RVCO (×5 mode: triangle; ×7 mode: square) and 5-stage RVCO (circle) versus the carrier frequency.

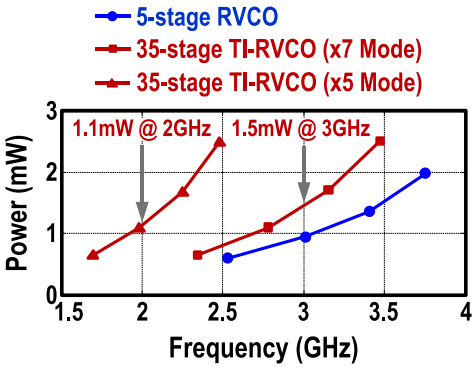

Fig. 19. Measured power consumption of the 35-stage dual-mode TI-RVCO (×5 mode: triangle; ×7 mode: square) and 5-stage RVCO (circle) versus the carrier frequency.

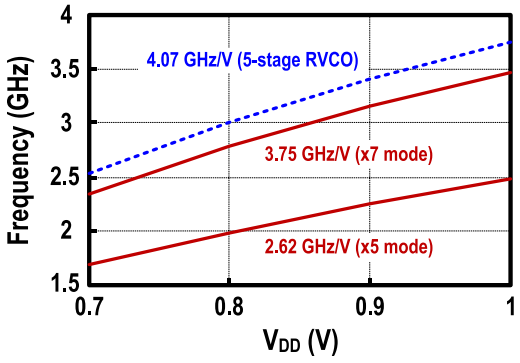

Fig. 20. Measured V_{DD}-to-frequency sensitivity. The 35-stage dual-mode TI-RVCO (solid line) at ×7 mode is close to that of the 5-stage RVCO (dash line) for their similar output frequency.

TABLE III
PERFORMANCE SUMMARY AND COMPARISON

	3 Prototypes Fabricated in This Work				C. Zhai et. al. VLSI'14 [18]	M. Kim et. al. JSSC'16 [19]	L. Kong et. al. JSSC'16 [3]
Technique	**35-Stage Dual-Mode TI-RVCO**		15-Stage TI-RVCO	Typical 5-Stage RVCO	RVCO + N-Path Filter	Current-Starved RVCO	RVCO Using Varactor for Freq. Tuning
Frequency Range (GHz)	1.7 to 3.47 (68.5%)		2.35 to 3.41 (36.8%)	2.53 to 3.75 (38.9%)	0.3 to 1.2 (120%)	1.2 to 2.0 (50%)	2 to 3 (40%)
Carrier (GHz) @ V_{DD}	1.7 @ 0.7V	3.47 @ 1V	3.41 @ 1V	3.75 @ 1V	1.0 @ 1.2V	1.6 @ 1.2V	2.4 @ 1V
1/f^3 PN Corner (kHz)	**90**	**150**	340	930	6000 [1]	700 [1]	4000 [1]
Power (mW)	0.65	2.51	2.25	1.99	4.7	1.1	3.1
PN @ 10kHz (dBc/Hz)	−49.7	−46.3	−43.7	-37.8	N/A	−22.9 [1]	N/A
PN @ 100kHz (dBc/Hz)	−77.6	−74.9	−73.6	−68.7	−80 [1]	−52.8	−66 [1,2]
PN @ 1MHz (dBc/Hz)	−100.4	−98.7	−98.9	−96.3	−110	−79.1	−96 [1,2]
PN @ 10MHz (dBc/Hz)	−120.5	−119.3	−119.9	−118.2	−138.7 [1]	−95.7	−123 [1,2]
FoM @ 10kHz (dBc/Hz)	**156.2**	**153.1**	150.8	146.3	N/A	126.6 [1]	N/A
FoM @ 100kHz (dBc/Hz)	**164.1**	**161.7**	160.7	157.2	153.3 [1]	136.5	148.7 [1,2]
FoM @ 1MHz (dBc/Hz)	**166.9**	**165.6**	166.0	164.8	163.3	142.8	158.7 [1,2]
FoM @ 10MHz (dBc/Hz)	167	166.1	167	166.7	172 [1]	139.4	165.7 [1,2]
Inherent Frequency Divided Output	**÷ 5**	**÷ 7**	÷ 3	No	No	No	No
Core Area (mm^2)	**0.003**		0.00086	0.00024	0.015	0.0007	0.001 [3]
CMOS Technology	65nm		65nm	65nm	65nm	65nm	45nm

1. Estimated from PN plot; 2. Simulation results; 3. Estimated from die micrograph;

$$\text{FoM} = -\text{PN} + 20\log_{10}(f_0/\Delta f) - 10\log_{10}(P_{DC}/1\text{mW})$$

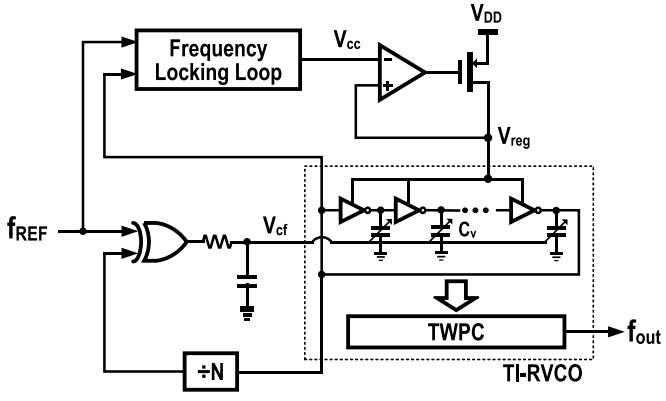

Fig. 21. A possible architecture for the TI-RVCO based type-I PLL.

Fig. 22 shows the measured output spurs within the frequency offset $f_o \pm 2f_o/7$ for $\times 7$ mode and within the frequency offset $f_o \pm 2f_o/5$ for $\times 5$ mode, which are < -43.1 dBc and < -37.9 dBc at the carrier frequencies of 3.47 and 2.48 GHz, respectively. Three samples have been measured and the average spurs are < -42 dBc and < -37 dBc at 3.47 and 2.48 GHz, which is higher than the simulated one of 50 dBc only considering random mismatch because of the presence of the deterministic mismatch.

The performance of the proposed TI-RVCO is compared with a typical RVCO as well as the prior art in Table III. Benchmarking with a typical 5-stage RVCO, the 35-stage dual-mode TI-RVCO reduces the f_{1/f^3} by $6.2\times$ at 3.47 GHz, which results in an improvement of FoM @ 10 kHz/100 kHz/1 MHz by 6.8 dB/4.5 dB/0.7 dB, respectively. Likewise, when contrasted with the RVCO + N-path filter technique [18], our TI-RVCO achieves $> 40\times$ lower f_{1/f^3}, 10 dB better FoM@100 kHz offset, and $5\times$ smaller die area. When compared with the current-starved RVCO [19], our TI-RVCO achieves $>4.6\times$ lower f_{1/f^3}, 25 dB better FoM@100 kHz offset at the cost of $4.3\times$ larger die area. The TI-RVCO, inherently offering a divided-by-M output, can benefit the type-I PLL [3] in terms of power and phase noise over a wide

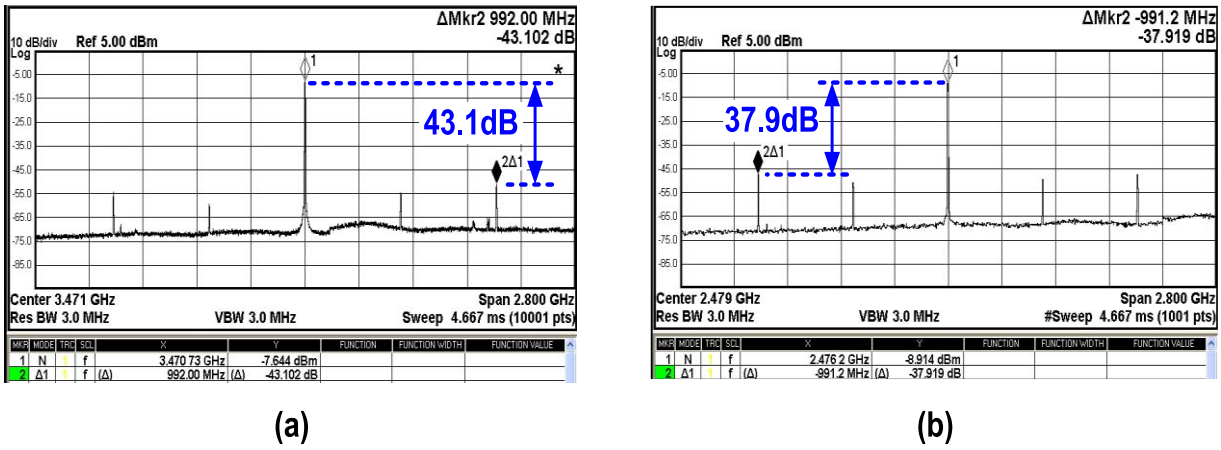

Fig. 22. Measured mismatch-induced output spurs of the 35-stage dual-mode TI-RVCO at the carrier frequency of (a) 3.47 GHz (×7 mode) and (b) 2.48 GHz (×5 mode).

range of frequency offsets, resulting in a better overall jitter performance.

VI. Conclusion

A TI-RVCO that has a significantly reduced f_{1/f^3} is presented. It also features a dual-mode operation according to the TI factors to extend the tuning range and generate an inherent divided output. A time-windowed phase combiner effectively recovers the high-frequency output with low extra delay offset and mismatch. The achieved FoM @ 10 kHz/100 kHz/1 MHz is 6.8 dB/4.5 dB/0.7 dB better than those of a typical RVCO, which results in the low $1/f^3$ phase noise corners from 90 to 150 kHz.

Appendix

This Appendix derives the expressions for $\Gamma^2_{rms,NMOS}$, $\Gamma^2_{DC,NMOS}$, $\Gamma^2_{rms,PMOS}$ and $\Gamma^2_{DC,PMOS}$ for NMOS and PMOS current noise. By approximating the ISF for the output nodes of a typical N-stage inverter-based RVCO in Fig. 23(a) as a triangular form, and assuming its peak value and width are inversely proportional to the maximum slope of the rising or falling edges [1] as shown in Fig. 23(b), $\Gamma^2_{rms,PMOS}$ and $\Gamma^2_{DC,PMOS}$ can be calculated as:

$$\Gamma^2_{rms,PMOS} = \frac{1}{\pi}\int_0^{\frac{1}{k_{max,r}}} \phi^2 d\phi = \frac{1}{3\pi}\cdot\left(\frac{1}{k_{max,r}}\right)^3 \quad (18)$$

$$\Gamma^2_{DC,PMOS} = \left(\frac{1}{\pi}\int_0^{\frac{1}{k_{max,r}}} \phi d\phi\right)^2 = \frac{1}{4\pi^2}\cdot\left(\frac{1}{k_{max,r}}\right)^4 \quad (19)$$

where $k_{max,r}$ is the maximum slope of the normalized rising edge. By replacing the $k_{max,r}$ in (18) and (19) with the maximum slope of the normalized falling edge $k_{max,f}$, $\Gamma^2_{rms,NMOS}$ and $\Gamma^2_{DC,NMOS}$ can also be obtained.

By further assuming that the single-stage delay τ is proportional to the total transition time of the rising and falling edges [1], i.e., $\tau_r = \eta/k_{max,r}$ and $\tau_f = \eta/k_{max,f}$, where η is the proportionality constant, the relationship between $k_{max,r}$ and the number of stages N can be obtained by satisfying the phase condition for oscillation, i.e., $N(\tau_r + \tau_f) = 2\pi$:

$$\frac{1}{k_{max,r}} = \frac{2\pi}{N\eta(1+\lambda)} \quad (20)$$

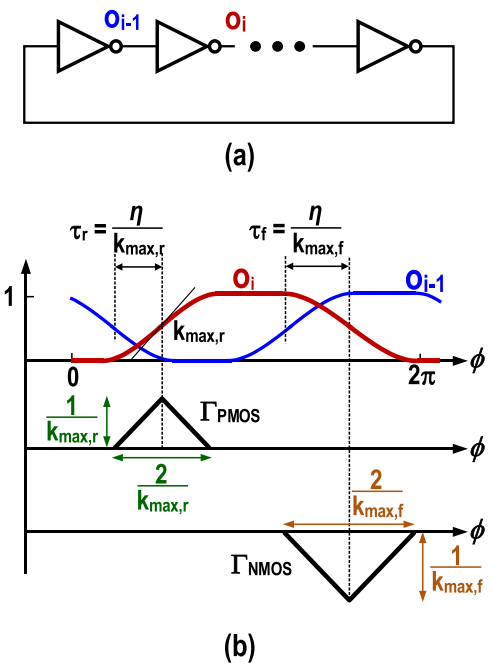

Fig. 23. (a) An inverter-based N-stage RVCO and (b) the corresponding waveforms and ISFs at its o_i.

where $\lambda = k_{max,r}/k_{max,f}$ is the ratio between the maximum slope of the normalized rising and falling edges as shown in Fig. 23(b). Replacing the $1/k_{max,r}$ in (18) and (19) with (20), the relationship between $\Gamma^2_{rms,PMOS}$, $\Gamma^2_{DC,PMOS}$ and the number of stages N can be obtained as:

$$\Gamma^2_{rms,PMOS} = \frac{8\pi^3}{3\eta^3(1+\lambda)^3}\cdot\frac{1}{N^3} \quad (21)$$

$$\Gamma^2_{DC,PMOS} = \frac{4\pi^2}{\eta^4(1+\lambda)^4}\cdot\frac{1}{N^4}. \quad (22)$$

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