Nano-Ampere Low-Dropout Regulator Designs for IoT Devices

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***Abstract*— This paper presents two output-capacitor-free low-dropout regulators (LDOs) with nA quiescent current for Internet-of-Things (IoT) applications. The proposed LDO1 combines the dynamic current biasing and the adaptive current biasing techniques for drastically reducing the quiescent current to the nA level while achieving fast transient response. Based on LDO1, the proposed LDO2 adds an inverter-based dynamic loop to further improve the transient response. The prototypes are fabricated in a 65-nm low-leakage CMOS process, with active areas of 0.0042 and 0.0048 m^2, respectively. Measurement results show that LDO1 and LDO2 consume 30 and 100 nA quiescent current, respectively, with 1 V input, 0.8 V output, and 100 nA load current. Stability analysis shows that both LDOs achieve good stability with load current ranging from 100 nA to 10 mA. With the load current steps from 100 nA to 10 mA in 1-μs transition time, the measured voltage undershoots are 336.8 mV for LDO1 and 196 mV for LDO2. Therefore, we reach a figure-of-merit of 0.00159 ps.**

***Index Terms*— LDO regulator, output-capacitor-free LDO regulator, ultra-low quiescent LDO, dynamic current boosting.**

I. Introduction

LOW dropout regulators (LDOs) are essential components in power management unit (PMU) designs for supporting widely distributed voltage domains [1], for noise-sensitive analog/RF circuits [2], and/or for the dynamic voltage scaling function in digital circuits [3]. An energy-efficient internet-of-things (IoT) device usually operates in the standby mode (idle state) for the majority of time, and is active only for a very short time interval [4]. Consequently, its power supply should cater for this special requirement to prolong the battery life. In other words, the quiescent current (I_Q) of the voltage regulators in the nA level is highly favorable. In addition, these LDOs need to support a fast transient response during the state transition period and provide good dynamic performance in the active mode [5]–[7]. However, the LDO with nA-level bias current only has a unity-gain bandwidth of tens of kHz, which can barely respond to the load and the input variations.

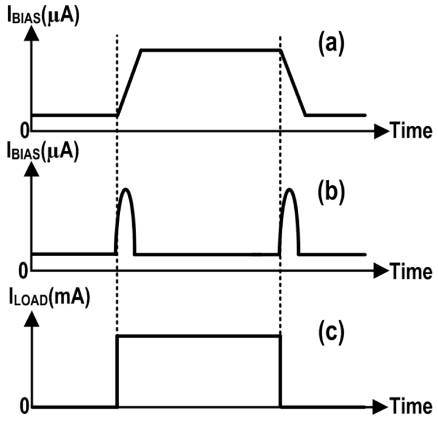

Fig. 1. Concept of non-static biasing techniques: (a) adaptive biasing technique [10], (b) dynamic biasing technique [11], [12], and (c) the loading step.

In prior works, several techniques were proposed to improve the transient response while keeping a low quiescent current. References [8] and [9] introduced advanced compensation techniques to control the damping factor of the closed-loop transfer function, for achieving a high GBW with a small I_Q and a small on-chip compensation capacitor. However, these LDOs usually have a limitation on the minimum load current (I_{LOAD}) for the stability issue, which raises the standby current (the summation of I_Q and I_{LOAD}). Meanwhile, the adaptive biasing technique [10], as Fig. 1(a) illustrates, was proposed to adjust the LDO bias current according to the load condition for stability considerations. As a result, the regulator can offer good dynamic performance in heavy I_{LOAD} while saves energy in the idle state. However, it can hardly help the transient response speed, because the quiescent current and consequently the loop bandwidth is still low at the beginning of the light-to-heavy load transient step.

As shown in Fig. 1(b), [11] and [12] introduced the dynamic biasing technique to alleviate the power-speed tradeoff further. Unlike that in Fig 1(a), dynamic biasing technique achieves fast-transient by only boosting the bias current during the transition period. In steady state, the bias current remains low.

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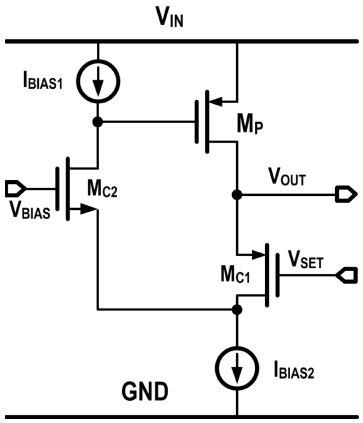

Fig. 2. Basic LDO structure based on the FVF topology.

Nevertheless, the dynamic biasing technique fails to provide good power supply rejection (PSR) in the active mode.

In this research, we propose two nA low dropout regulators that combine adaptive biasing and dynamic biasing techniques. Both of them can provide fast transient response and good power supply rejection (PSR) at full loading conditions.

The organization of this paper is as follows: Section II introduces the circuit implementation, including the architectural consideration, the proposed scheme, overall circuit diagram, as well as the stability and the PSR analysis. Section III shows the measured transient and PSR performances, and compares our work with the state-of-the-art. Finally, Section IV draws the conclusions.

II. Circuit Implementations

In this section, we will present two nA output-capacitor-free LDOs, denoted as LDO1 and LDO2, combining the adaptive biasing and the dynamic biasing techniques. Firstly, we will discuss the architectural considerations. Then, we will provide the stability analysis, the full schematic and the simulated transient performance.

A. Architectural Considerations

Fig. 2 shows a simplified LDO structure [13] based on the flipped-voltage-follower (FVF) topology. In this scheme, M_{C1} and M_{C2} form a folded-cascode common-gate amplifier which acts as the error amplifier (EA). Since the FVF is a single-ended topology, for a similar dynamic response, the FVF-based LDO only costs about 50% current compared to a conventional differential EA [14]. As a result, FVF-based LDOs are preferably used in low-power applications like IoT. On the other hand, poor DC regulation of the FVF-based LDO should be improved for higher accuracy. Therefore, [2] acquired better DC accuracy by introducing a tri-input EA, while [15] added a non-inverting second stage to obtain 20-30 dB extra loop gain. Consequently, we chose the FVF topology as our starting point.

B. Structure of the Proposed Transient Enhancement Circuit

Fig. 3 illustrates the basic structure and operation principle of the proposed LDO1 and LDO2. To be specific, the main

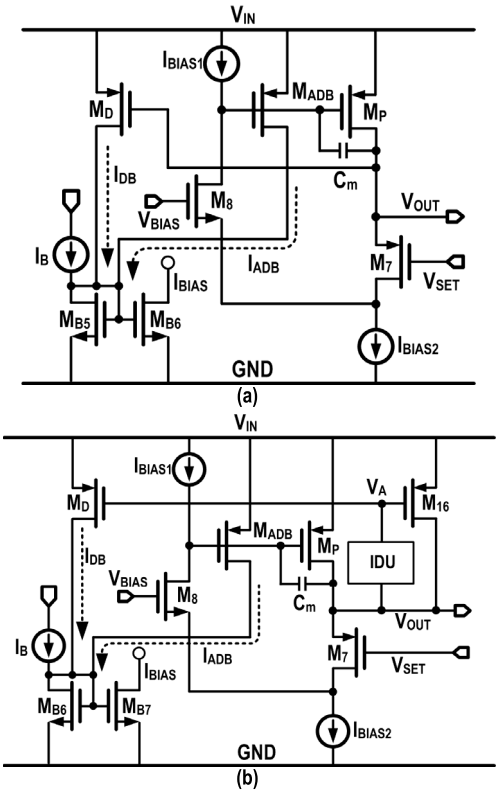

Fig. 3. Proposed structure of the (a) LDO1 and (b) LDO2 with hybrid basing scheme.

TABLE I
Sizes of the Core Transistors

LDO1	M_{B5}	M_{B6}	M_7	M_8	M_D	M_{ADB}	M_P	
Size (μm)	2/1	2/1	2×5/1	2×5/1	6×0.5/0.06	0.4/0.06	1000×0.4/0.06	
LDO2	M_{B6}	M_{B7}	M_7	M_8	M_D	M_{ADB}	M_P	M_{16}
Size (μm)	2/1	2/1	2×5/1	2×5/1	4×0.08/0.06	0.4/0.06	1000×0.4/0.06	10×0.08/0.06

design parameters are summarized in Table I. The main features of these two schemes are the adaptive biasing and the dynamic biasing. As Fig. 3 shows, with the same adaptive biasing loop in LDO1 and LDO2, I_{ADB} is linearly adjusted according to I_{LOAD} by a ratio of 1:1000 between the auxiliary transistor M_{ADB} and the output power transistor M_P, for the tradeoff between low quiescent current and good dynamic performance. To be specific, once the output stage delivers more power, I_{BIAS} will be boosted up simultaneously. Consequently, a larger I_{BIAS} broadens the unity-gain bandwidth (UGB) and enlarges the slew-rate at the gate of M_P. When I_{LOAD} is at the maximum value (10mA), this adaptive loop provides $I_{ADB} = 12\ \mu A$ in our designs.

On the other hand, the dynamic loops for LDO1 and LDO2 are different. As Fig. 3(a) illustrates, the gate of the transistor M_D for the dynamic loop is directly connected to V_{OUT} in LDO1. During the transient state, M_D converts the V_{OUT} droop into a dynamic bias current I_{DB}. When the load transient ends, I_D keeps a low value to save energy. In a more advanced version, Fig. 3(b) introduces a fast transient-enhancement loop for LDO2, including an inverter-based

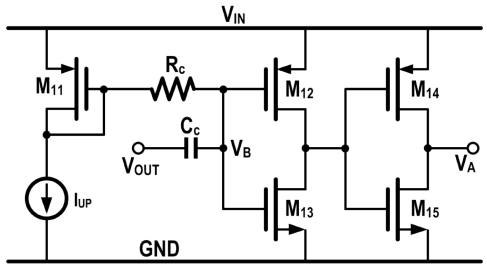

Fig. 4. Inverter-based dynamic unit (IDU) with trip point calibration.

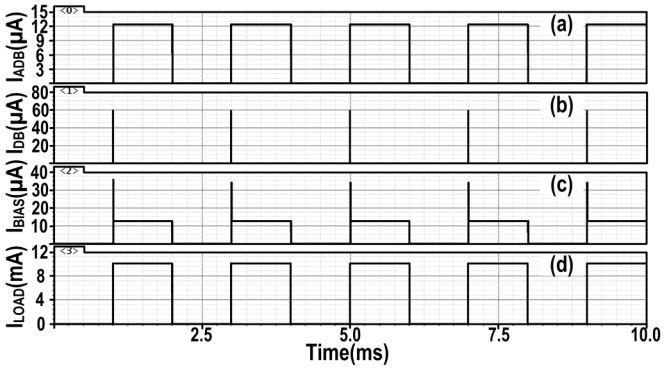

Fig. 5. Simulated currents of (a) M_{ADB} with adaptive biasing technique, (b) M_D with dynamic biasing technique, (c) M_{B7} with hybrid biasing scheme, and (d) the load step with 1 μs edge time.

dynamic unit (IDU) and a transistor M_D. When the load transient occurs, the induced voltage droop will be firstly detected by the IDU and then transferred into a dynamic I_{DB} through M_D with little loop latency.

To accommodate the process variations and improve the design robustness, Fig. 4 shows the implementation of the IDU with a simple trip-point calibration scheme. The coupling capacitor C_C serves as a high-pass path, which couples the V_{OUT} droop to V_B. I_{UP} is employed to provide a DC operating point for M_{12} and M_{13}. A 10-kΩ Rc is inserted to block the disturbance from C_C to M_{11}. Generally, this dynamic loop functions for two purposes. Firstly, it detects the V_{OUT} droop in the transient state and then creates a dynamic bias current I_{DB}. To improve the detection sensitivity, the trip point of the first inverter is set to be close to V_{OUT}. Furthermore, the second inverter acts as an amplifier to generate a sharp edge on V_A. Secondly, in steady state, the IDU acts as a switch that entirely turns off M_D to further reduce the static power dissipation.

Fig. 5(a) illustrates the relationship between I_{ADB} and I_{LOAD} for LDO2. When I_{LOAD} is 100nA, I_{ADB} is merely 1 nA, and then I_{ADB} is adjusted to 12 μA when I_{LOAD} is 10 mA. Fig. 5(b) outlines a dynamic current pulse I_{DB} in the transient period. A dynamic current pulse I_{DB} of maximum 58 μA is immediately generated within a narrow time interval. The steeper the loading step is, larger and longer the magnitude and duration of this dynamic current pulse will be. Finally, Fig. 5(c) exhibits the total I_{BIAS} with the hybrid biasing techniques. The adaptive and dynamic I_{BIAS} with different DC and AC I_{LOAD} shows an event-driven-like characteristic, thus enabling an energy-efficient operation of this LDO.

C. Circuit Implementation

Fig. 6(a) and 6(b) present the full schematic of the proposed LDO1 and LDO2, respectively. For both LDOs, the EA is constructed by M_6 through M_{10}. C_1 is implemented by dummy transistors to suppress the noise. Besides, C_m of 500 fF and C_2 of 400 fF are obtained with N-type MOS capacitors to stabilize the structure and to filter the noise. In addition, M_1 through M_5 form an auxiliary differential EA, which serves as a control voltage generator.

For LDO1, M_D serves for the dynamic loop. Specifically, when V_{OUT} suddenly drops due to an urgent I_{LOAD} request, the gate-source voltage of M_D increases simultaneously and thus leads to more bias current. To ensure a low static current dissipated by this dynamic loop, M_D is implemented with a high-threshold-voltage transistor. In heavy load condition, I_{ADB} will dominate the bias current, and therefore ensures the LDO1 with good dynamic performance in the active state. The total quiescent current of LDO1 is only 60 nA (simulated) in idle state.

For LDO2, the transient performance has been further improved with the inverter-based dynamic loop when compared with LDO1. Here, we use a $C_C = 3$ pF to sense the high frequency voltage spikes in the transient period. The V_{OUT} variations will be amplified by the two inverters, producing a narrow voltage pulse at the gates of both M_D and M_{16}. Then, the large voltage pulse activates M_D and M_{16} to provide a large I_{DB} pulse and specific output transient current. Consequently, the generated dynamic bias current in LDO2 is much larger than that in LDO1 (1.5 μA in LDO1 and 58 μA in LDO2) with the load current transiting from 100 nA to 10mA within 1 μs. As aforementioned, the inverter-based transient enhancement unit will fully turn off M_D in the idle state to further reduce I_Q.

Moreover, M_{16} acts as an ultra-fast compensation loop, because the resultant dynamic current of M_{16} directly compensates the I_{LOAD} to improve the V_{OUT} droops. The IDU and M_D form a high-gain fast loop with reduce the dynamic stability for fast transient droop reduction, while the IDU with M_{16} form a low-gain fast loop that reduces the V_{OUT} peaking during load transient period. So, the transient performance with dynamic biasing is a joint effort of M_D and M_{16}. Fig. 7 shows the transient responses with different size ratios of $(W/L)_D$:$(W/L)_{16}$ = 4:0, 4:10, 2:10, and 4:20, respectively. Apparently, a larger M_{16} helps to avoid the serious voltage peaking which is caused by the reduced stability of using large dynamic biasing current. As a result, we can observe a transient V_{OUT} groove. To make a compromise between the contribution from M_{16} and M_D, we adopt $(W/L)_D$:$(W/L)_{16}$ = 4:10 in this design.

Fig. 8 shows the simulated load transient responses of the proposed LDO1 and LDO2, while comparing them with a baseline design without the dynamic loop. With the same 1 V supply voltage and 10 pF load capacitor, Fig. 8(a), (b), and (c) give the corresponding transient response with these three schemes for the I_{LOAD} steps from 100 nA and 10 mA within

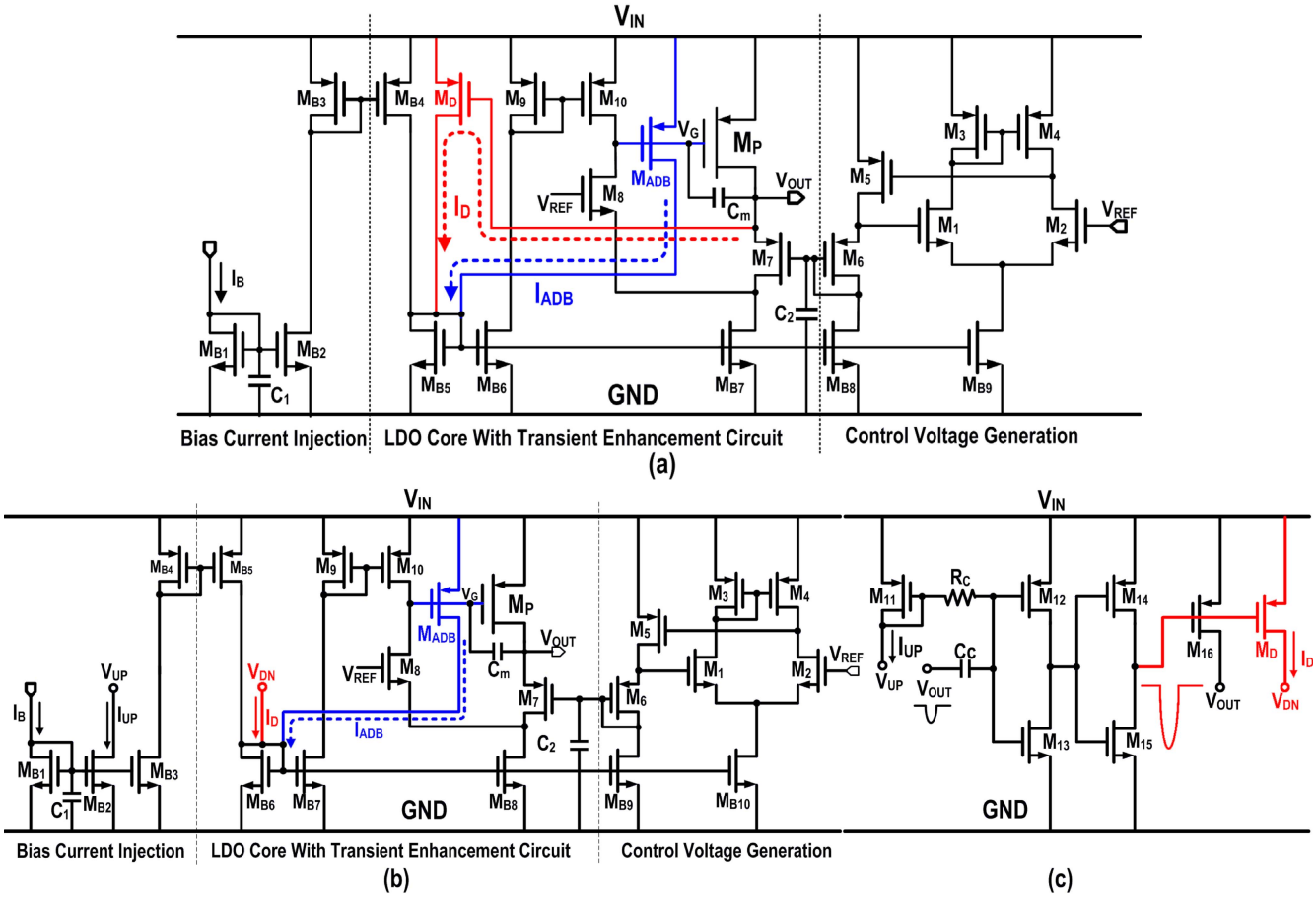

Fig. 6. Full schematic of the proposed (a) LDO1; (b) LDO2 core; and (c) inverter-based transient enhancement unit in LDO2 with trip point calibration.

500 ns, 100 ns, and 20 ns, respectively. In the 500-ns edge time case, the undershoots for LDO1, LDO2, and the baseline design are 360 mV, 191 mV, and 600 mV, respectively. The maximum undershoot improvement from LDO2 is 409 mV. With an edge time of 100 ns, the undershoots for LDO1, LDO2 and the baseline design are 520 mV, 290 mV and 720 mV, respectively. When the edge time is 20 ns, although all the LDOs cannot respond fast enough to the load transient, LDO2 reduces the settling time by more than four times compared to the baseline design.

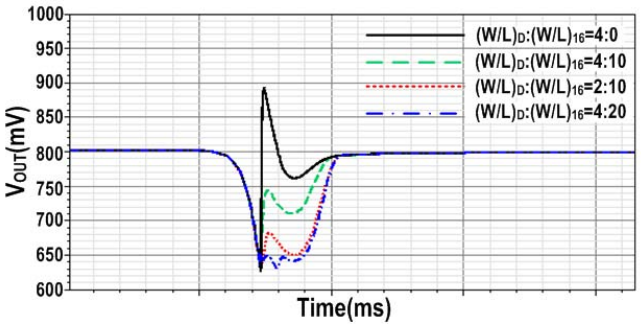

Fig. 7. Simulated load transient response with different $(W/L)_D$: $(W/L)_{16}$ for a 100 nA – 10 mA rising load step with 1 μs edge time.

D. Stability Analysis

We use Miller compensation in the proposed structures with the targeted load capacitance range of below 10 pF, and the minimum I_{LOAD} can be lowered down to several tens of nA. We set the dominant pole at the gate of M_P. As the adaptive and dynamic biasing circuits only affect the DC operating points of the LDO, we may ignore them in the small-signal model. Fig. 9 gives the small-signal model for both LDO1 and LDO2, where R_{O1} and C_{P1} are the equivalent

$$A_v = \frac{v_{out}(s)}{v_{in}(s)} = \frac{A_{dc}(1 - sC_m/g_{mp})}{1 + s[(C_{OUT}+C_m)R_{OUT} + (C_{P1}+C_m)R_{O1} + C_m g_{mp} R_{O1} R_{OUT}] + s^2 R_{O1} R_{OUT}(C_{P1}C_{OUT} + C_{P1}C_m + C_{OUT}C_m)}, \quad (1)$$

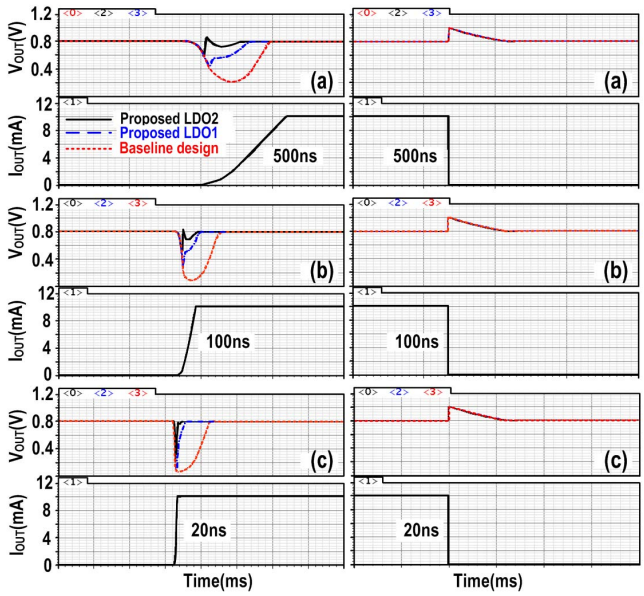

Fig. 8. Simulated load transient responses of LDO1, LDO2, and a baseline design, when the load transient edge time is (a) 500 ns, (b) 100 ns, and (c) 20 ns, respectively.

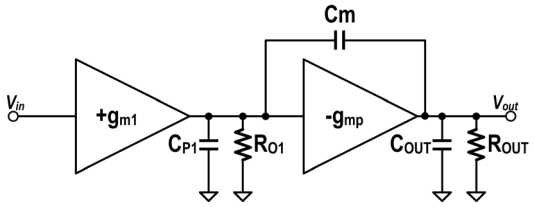

Fig. 9. Small-signal modelling of the proposed LDO.

output resistance and lumped parasitic capacitance of the first stage, respectively. R_{OUT} is the equivalent resistance on the LDO output node including the load resistance in parallel, and C_{OUT} includes the parasitic capacitances from the LDO and the loading circuits. With the assumption of $g_{mp}\ R_{OUT} \gg 1$, $g_{m1}\ R_{O1} \gg 1$, $C_{OUT} \gg C_m > C_{P1}$, and other negligible inter-stage coupling capacitances, the transfer function of the proposed LDOs is given as (1), as shown at the bottom of the previous page, and the poles and the zero become

$$P_0 \approx -\frac{1}{C_m R_{O1} g_{mp} R_{OUT}}, \tag{2}$$

$$P_1 \approx -\frac{g_{mp}}{C_{OUT}(1+\frac{C_{P1}}{C_m})}, \tag{3}$$

$$Z = \frac{g_{mp}}{C_m}, \tag{4}$$

where $A_{dc} = g_{m1}R_{O1}g_{mp}R_{OUT}$ is the low-frequency open-loop gain, P_0, P_1, and Z represent the dominant pole, the non-dominant pole and a right-half-plane zero. To ensure the closed-loop stability, we use a Miller capacitor $C_m = 500$ fF to push P_0 to low frequency at the minimum I_{LOAD}. Meanwhile, we design P_1 to be at least 2× higher than P_0 to improve the phase margin (PM). Also, we locate P_1 at a lower frequency than Z with $C_{OUT} = 10$ pF, to obtain a good gain margin.

Fig. 10 shows the simulated Bode plots of the proposed LDO2 at different I_{LOAD} with 10 pF output capacitance. The highest DC loop gain reaches 73 dB while the worst case of 31 dB occurs at $I_{LOAD} = 100$ nA with PM = 45°. In addition, once I_{LOAD} is larger than 10 μA, simulation results show at least 78° phase margin, which verifies the good stability of these compensated structures.

E. Power Supply Rejection

Since both LDOs have the same EA topology and the adaptive biasing loop, their PSR performances are very similar. We may use the simplified small-signal model shown in Fig. 11 for the PSR analysis. Where A(s) is the open-loop gain of the EA. Then, the PSR transfer function can be expressed as (5), as shown at the bottom of this page.

At low frequency, this equation can be simplified as:

$$PSR_{f-low} \approx \frac{1}{A(s)(1+\frac{C_{gsp}}{C_m})}. \tag{6}$$

With a relatively large loop gain, a good $PSR_{f\text{-}low}$ can be achieved. Besides, the parasitic C_{gsp} of M_P tends to couple Vdd to the gate of M_P, which also helps to improve $PSR_{f\text{-}low}$. However, the PSR starts to become worse when the frequency approaches the dominant pole (P_0) of the loop, as the loop gain drops [22], [23]. When the frequency approaches the unity-gain frequency (UGF), the PSR is mainly determined by the passive components. The UGF of this topology is given as:

$$UGF = \frac{g_{m1}}{C_m}. \tag{7}$$

Obviously, a larger biasing current I_{ADB} helps to increase g_{m1} and thus extends the good PSR range to a higher frequency. A larger C_m will make M_P acting more like a diode-connected transistor, passing the supply noise to the output. Therefore, a small C_m is preferable when the stability requirement is satisfied. At high frequency, C_{OUT} tends to be a "short circuit" to bypass the noise on the output node and improves the high frequency PSR.

III. Measurement Results

The proposed two output-capacitor-free nA LDOs have been fabricated in a 65-nm low-leakage CMOS process. Fig. 12(a) shows the chip micrographs. The active silicon areas for LDO1 and LDO2 are 0.0042 mm^2 (98 μm × 43 μm) and 0.0048 mm^2 (120 μm × 40 μm), respectively, excluding the pads. Both LDOs deliver a 10-mA maximum I_{LOAD} with a nominal V_{OUT} of 0.8 V under a supply of 1 V. Fig. 12(b)

$$PSR = \frac{V_{out}}{V_{dd}} = \frac{sC_{gsp}C_m R_{OUT} r_{dsp} + C_m g_{mp} R_{OUT} r_{dsp} + (C_{gsp}+C_m)R_{OUT}}{A(s)R_{OUT} r_{dsp}(C_{gsp}+C_m)(g_{mp}-sC_m) + sR_{OUT} r_{dsp}(C_{gsp}+C_m)(C_{OUT}+C_m+C_{gsp} \parallel C_m) + (r_{dsp}+R_{OUT})(C_{gsp}+C_m) - C_{gsp} g_{mp} R_{OUT} r_{dsp}} \tag{5}$$

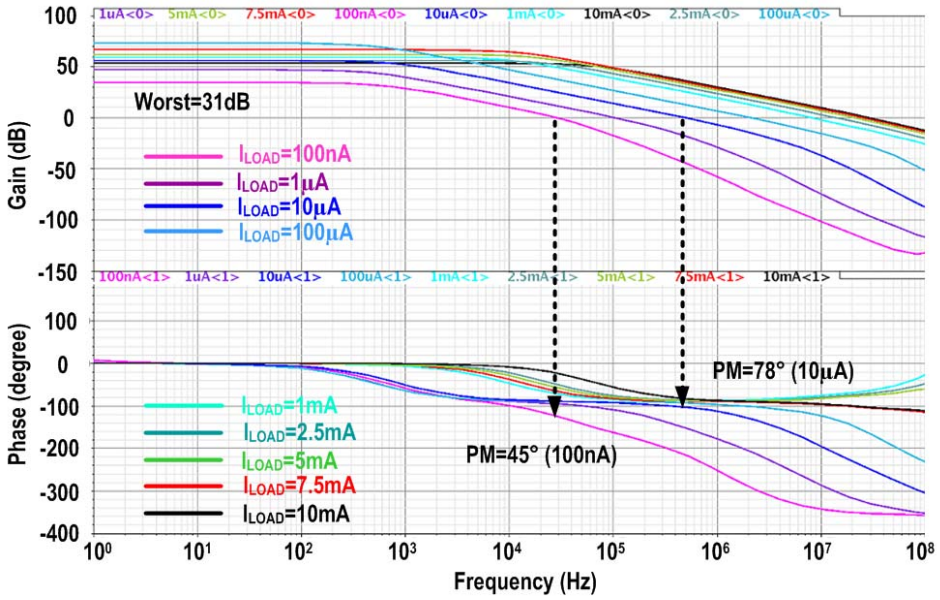

Fig. 10. Simulated Bode plots of the proposed LDO2 with different I_{LOAD} and C_{OUT} = 10 pF.

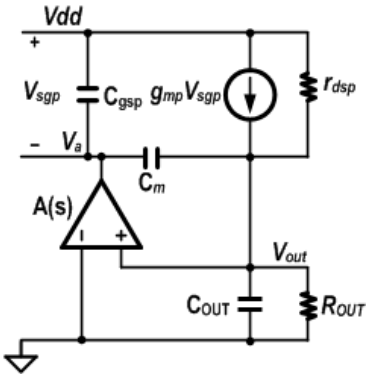

Fig. 11. A simplified small-signal model for the PSR analysis.

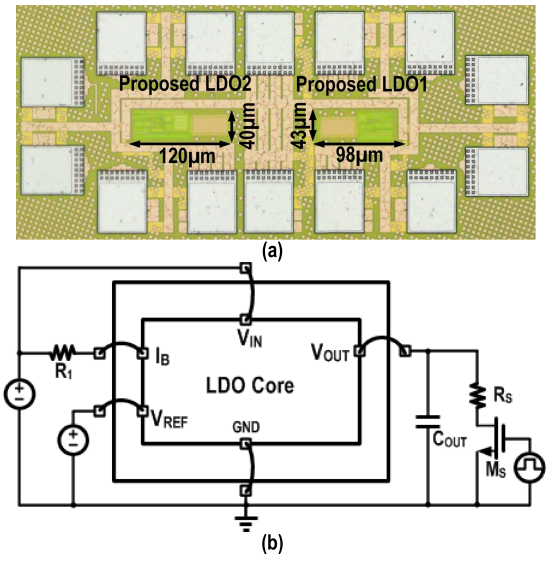

Fig. 12. (a) The micrographs and (b) the measurement setup of the proposed LDO1 and LDO2.

presents the measurement setup for both LDOs. For simplicity, R_1 is realized off-chip to generate a 10 nA bias current. Meanwhile, C_{OUT}, M_S, and R_S are also implemented on the PCB for load transient measurements.

Fig. 13–16 show the measured load transient waveforms of V_{OUT} for both LDO1 and LDO2, with the load transient step changes from 100 nA to 10 mA with different edge times. Both LDOs, with and without the proposed dynamic biasing techniques, have been measured.

Fig. 13 shows the transient voltage undershoots and overshoots of the proposed LDO1, when I_{LOAD} changes from 100 nA to 10 mA within 1 μs. The left column shows the transient waveforms of the proposed LDO1, whereas the right column shows it without the dynamic biasing loop. With the measured quiescent current of 30 nA in the idle state, the measured undershoot and overshoot without the dynamic biasing loop are 548.2 mV and 163.6 mV, respectively. When the dynamic loop is activated, the undershoot and overshoot decrease to 336.8 mV and 163.2 mV, respectively, with more than 200 mV improvement on the undershoot. For the heavy-to-light load transition, the overshoot voltage is naturally discharged by the tiny light-load current, which means the over-charged energy on C_{OUT} is used by the load and is not wasted.

Fig. 14 shows the measured transient performance of LDO2. With the same measurement setup and load transient current as in the LDO1, the measured undershoots with and without the inverter-based dynamic loop are 196 mV and 538 mV, respectively.

Fig. 15 shows the measured voltage undershoots of LDO1 and LDO2 with I_{LOAD} changing from 100 nA to 10 mA within 200 ns. In this case, the undershoot has been minimized from 715.1 mV to 487.5 mV for LDO1, and from 710.9 mV to

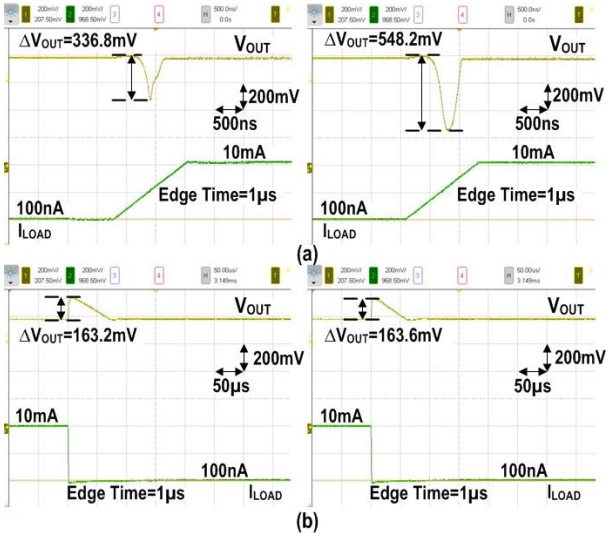

Fig. 13. Measured load transient voltage (a) undershoot and (b) overshoot of LDO1 with $V_{IN} = 1$ V, $V_{OUT} = 0.8$ V, $C_{OUT} = 10$ pF, and 1-μs edge times, with (left) and without (right) the proposed dynamic biasing technique.

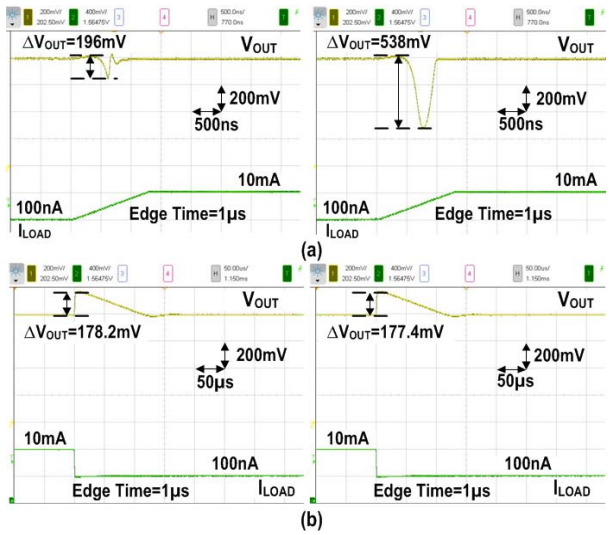

Fig. 14. Measured load transient voltage (a) undershoot and (b) overshoot of LDO2 with $V_{IN} = 1$ V, $V_{OUT} = 0.8$ V, $C_{OUT} = 10$ pF, and 1-μs edge times, with (left) and without (right) the proposed dynamic biasing technique.

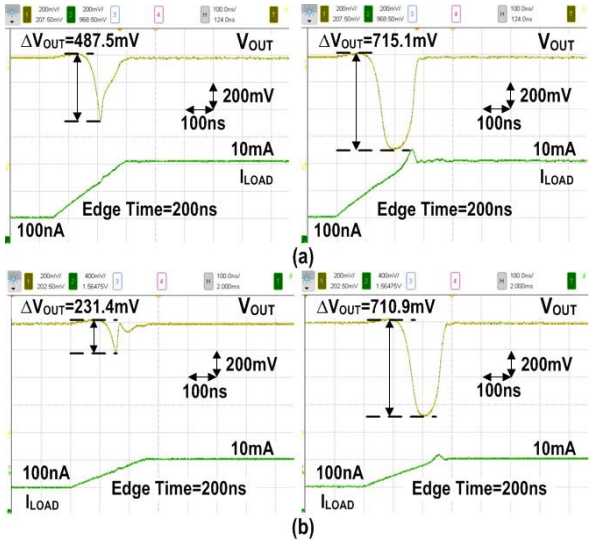

Fig. 15. Measured voltage undershoots for (a) LDO1 and (b) LDO2, with $V_{IN} = 1$ V, $V_{OUT} = 0.8$ V, $C_{OUT} = 10$ pF, and 200-ns edge time, with (left) and without (right) the dynamic biasing techniques.

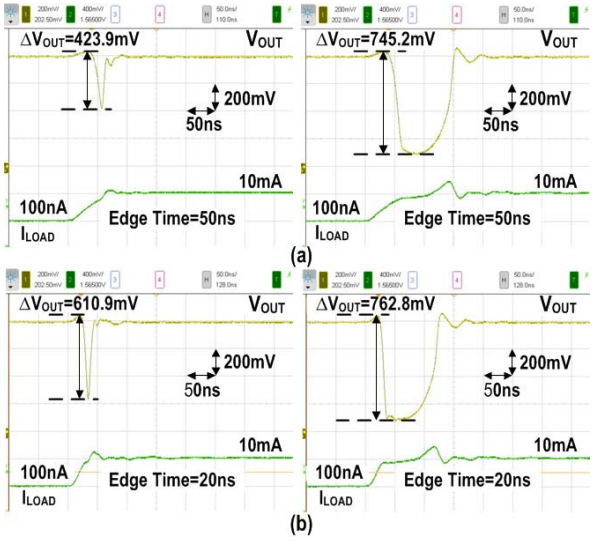

Fig. 16. Measured voltage undershoots of LDO2 with (left) and without (right) the inverter-based dynamic biasing scheme, with $V_{IN} = 1$ V, $V_{OUT} = 0.8$ V, $C_{OUT} = 10$ pF, and (a) 50-ns and (b) 20-ns edge times, respectively.

231.4 mV for LDO2, respectively. Meanwhile, V_{OUT} of both versions settles within 200 ns.

Fig. 16 shows the load-transient of LDO2 with an edge time of 50 ns and 20 ns, respectively. In these scenarios, we can still observe the undershoot improvements of 320 mV for the 50-ns edge time case and 150 mV for the 20-ns edge time case.

Monte Carlo simulations including the process variation and device mismatch have been conducted to validate the statistical performance of the proposed techniques. As Fig. 17(a) illustrates, LDO1 achieves an average quiescent current of 72.1 nA with a standard deviation of 13.6 nA for 200 samples. Similarly, Fig. 17(b) presents an average quiescent current of 153.5 nA with a standard deviation of 56.9 nA for LDO2. Meanwhile, Fig. 17(c) and Fig. 17(d) give the transient performance of LDO1 and LDO2 with 200 samples.

Fig. 18 exhibits the measured transient waveforms of LDO2 with input ripples at the frequencies of 200 kHz and 1 MHz for the PSR calculation at full load. Fig. 19 shows the summary of the measured PSR of LDO2 up to 40 MHz. The proposed LDO2 achieves a PSR of -28 dB at 300 kHz and a PSR of -24 dB at 1 MHz. The worst case PSR of 1.6 dB occurs at 30 MHz.

Fig. 20 depicts the measured I_Q versus I_{LOAD} and the DC load regulation of the proposed LDO1 and LDO2 with five samples. As Fig. 20(a) shows, the quiescent current of LDO1 increases in an almost linear way due to the adaptive biasing loop. It also reveals that LDO1 can regulate V_{OUT} when I_{LOAD} down to 0 nA. And, the worst I_Q is measured to be 30 nA when I_{LOAD} is 100 nA, while the maximum I_Q is 97 μA with $I_{LOAD} = 10.3$ mA. Among the five samples,

TABLE II
PERFORMANCE COMPARISONS

Publication	[2] 2015 TCAS-I	[11] 2010 JSSC	[12] 2007 TCAS-II	[13] 2005 JSSC	[15] 2010 JSSC	[16] 2013 TCAS-I	[17] 2013 TCAS-II	[18] 2016 ASSCC	[19] 2017 ISSCC	[20] 2017 ISSCC	[21] 2017 TPEL	Proposed LDO1	Proposed LDO2
Type	Analog	Analog	Analog	Analog	Analog	Analog	Analog	Hybrid	Hybrid	Analog	Analog	**Analog**	**Analog**
Technology	65nm	0.35μm	0.35μm	90nm	90nm	65nm	0.35μm	0.35μm	65nm	65nm	0.13μm	**65nm**	**65nm**
Active area(mm2)	0.0234	0.155	0.09	0.098	0.019	0.017	0.04	0.25	0.03	0.016	0.008	**0.0042**	**0.0048**
V_{DO}(mV)	150	200	100	300	250	200	200	200	50	50-150	200-600	**200**	**200**
V_{OUT}(V)	1	1.2	0.9	0.9	0.5	1	1	1.2-4.8	0.45-0.95	0.05-0.15	0.8	**0.8**	**0.8**
I_Q(μA)	50	43	1.2	6000	8	0.9-82.4	1.2-1.4	0.09	3.2	0.41	112	**0.03**	**0.1**
MAX I_{LOAD}(mA)	10	100	50	100	100	100	100	20	12	0.05	25	**10**	**10**
C_{LDO}(pF)	N/A	6	0	N/A	7	4.5	0	N/A	100	0.2	0.73	**0.9**	**3.9**
C_{OUT}(pF)	140	0-1000	100	600	0-50	100	100	1000	10	40	0-25	**10**	**10**
PSR(dB)	-15.5 1GHz	N/A	N/A	N/A	-44 1kHz	-17* 1MHz	N/A	-12* 10kHz	N/A	-22.9 1MHz	-57 1MHz	**-24 1MHz**	**-24 1MHz**
ΔV_{OUT}(mV)	82	70	450*	90	114	68.8	270	850	105	34.8	284	**487.5**	**231.4**
DC Load Reg. (mV/mA)	1.1	~0.4	0.148	1.8	0.1	0.3	N/A	0.9	N/A	~200	0.173	**1.22**	**1.58**
Settling time(μs)	0.05*	3	2.8	N/A	5	6	2.7	1.8	5*	20*	<0.2	**0.25**	**0.1**
Edge time(ns)	0.2	1000	1000*	0.1	100	300	1000*	1000	1	10000	0.3	**200**	**200**
Edge time ratio K	2	10000	10000*	1	1000	3000	10000	10000	10	100000	3	**2000**	**2000**
FOM_T**	5.74ps	N/A	67ps	32ps	0.00485ps	0.0006ps	0.00325ps	0.191ps	0.34ps	228.3ps	1.3ps	**0.00159ps**	**0.00322ps**
FOM_V***	0.00082*	0.304	0.108*	0.0054	0.0094	0.0019	0.0324*	0.038	0.00034	28.5	0.004	**0.0029**	**0.0046**

* Estimated from measured result ** $FOM_T = \frac{C_{TOT} \times \Delta V_{OUT}}{\Delta I_{LOAD}} \times \frac{I_Q}{\Delta I_{LOAD}}$ ($C_{TOT} = C_{LDO} + C_{OUT}$) *** $FOM_V = K \times \frac{\Delta V_{OUT} \times I_Q}{\Delta I_{LOAD}}$ (K is the edge time ratio compared to the smallest one in the table)

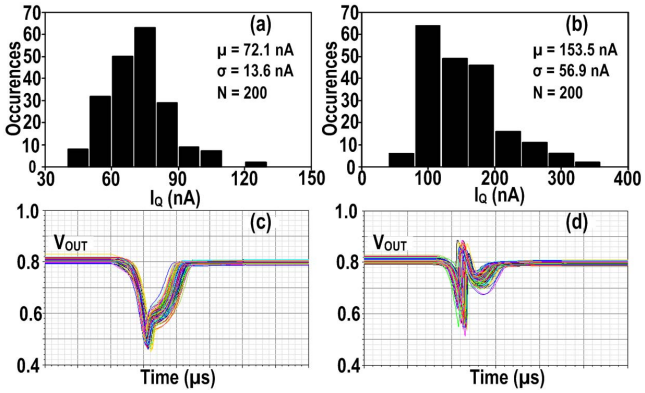

Fig. 17. Monte-Carlo simulation for (a) quiescent current of LDO1; and (b) quiescent current of LDO2; and the (c) undershoot of LDO1; and (d) undershoot of LDO2 with I_{LOAD} steps from 100 nA to 10mA within 1μs.

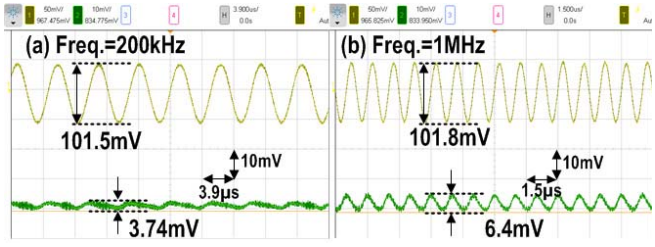

Fig. 18. Measured transient waveform of LDO2 at full load for the PSR calculation with input ripples at (a) 200 kHz and (b) 1 MHz, respectively.

the largest DC load regulation for LDO1 is 1.22 mV/mA. Similarly, Fig. 20(b) presents a linear function of the I_Q versus I_{LOAD} of LDO2. The measured worst case for I_Q is 100 nA

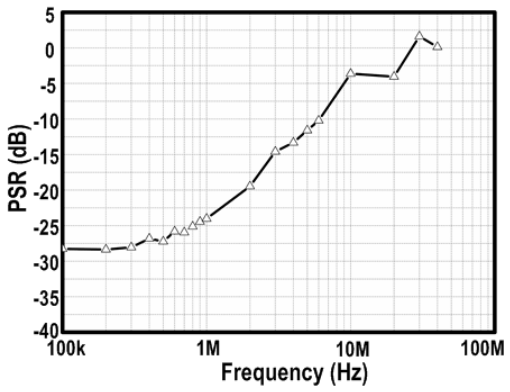

Fig. 19. Measured PSR versus frequency of the proposed LDO2 with $I_{LOAD} = 10$ mA, $V_{OUT} = 0.8$ V, and $C_{OUT} = 10$ pF.

when I_{LOAD} is down to 100 nA, and the maximum I_Q is 104 μA when $I_{LOAD} = 10.3$ mA. As a result, the worst DC load regulation for LDO2 is 1.58 mV/mA.

The measured performances of the proposed regulators are compared with the state-of-the-art in Table II. For comparing advanced LDOs, there are two widely-used figures-of-merit (FOMs) proposed in [13] and [15], classified as FOM_T and FOM_V. According to Table II, both proposed LDOs achieve competitive FOMs among recently reported works. Furthermore, the quiescent currents of 30 nA and 100 nA for the proposed LDO1 and LDO2, respectively, are the smallest reported. With the proposed LDO scheme that combines adaptive biasing and dynamic biasing, the LDO1 and LDO2 can

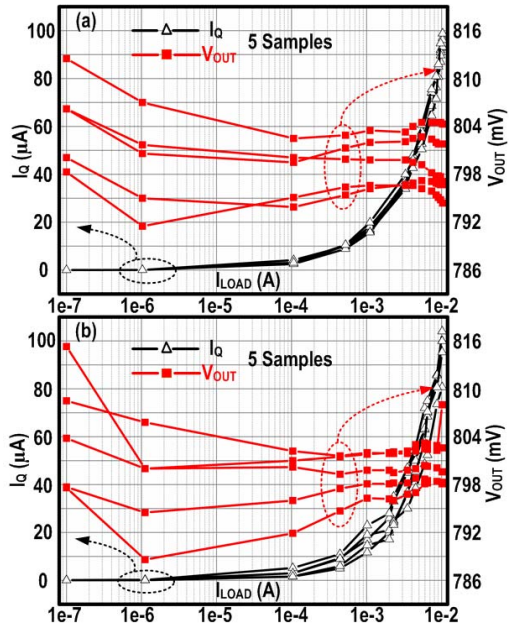

Fig. 20. Measured I_Q and V_{OUT} versus I_{LOAD} of (a) LDO1 and (b) LDO2.

provide fast-transient and good dynamic performance at heavy I_{LOAD}, with I_Q in the nA range.

IV. Conclusions

Ultra-low stand-by power voltage regulators are at high demand for IoT devices. To address this issue, two output-capacitor-free nA quiescent current LDOs have been proposed. We combined adaptive and dynamic biasing techniques to achieve better speed and power trade-off. Also, we proposed different circuit implementation techniques for these two LDOs, demonstrating similar but different performance features. The experimental verification of the prototypes uses a 65-nm low-leakage CMOS process with small active areas. With the introduced hybrid biasing scheme, these two proposed LDOs provide a driving capability of 10 mA under 1 V supply and 200 mV nominal dropout voltage. Measured results show significant transient improvements with an I_Q of 30 nA for LDO1 and 100 nA for LDO2. Meanwhile, both LDO1 and LDO2 provide a PSR of -24 dB at 1 MHz with full load. Compared to the prior-art works, the proposed regulators achieve the lowest quiescent current while largely improve the transient response, consequently attaining a good FOM_T of 0.00159 ps and 0.00322 ps, respectively.

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