An 11b 450 MS/s Three-Way Time-Interleaved Subranging Pipelined-SAR ADC in 65 nm CMOS

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***Abstract*—This paper presents an 11 bit 450 MS/s three-way time-interleaved (TI) subranging pipelined-successive approximation register (SAR) analog-to-digital converter (ADC). The proposed hybrid architecture combines the design benefits of different ADC structures to achieve a high conversion rate and accuracy with good power efficiency. The design employs multiple offset calibration schemes to compensate the offset mismatches at each stage. The solutions require less calibration efforts, thus allowing the ADC to achieve a compact area. Furthermore, a dynamic SAR controller embedded with error-decision-correction (EDC) logic is proposed to reduce large transition error. Measurement results on a 65 nm CMOS prototype operated at 450 MS/s and 1.2 V supply show 7.4 mW total power consumption with a peak signal-to-noise distortion ratio (SNDR) of 60.8 dB and an FOM of 32 fJ/conv.step at Nyquist.**

***Index Terms*—Offset calibration, pipelined-successive approximation register (SAR) analog-to-digital converter (ADC), SAR logic.**

I. Introduction

THE SUCCESSIVE approximation register (SAR) analog-to-digital converters (ADCs) [1]–[3] benefit from their simple configuration and mostly dynamic operation exhibiting excellent power and area efficiency under technology down scaling, while the sequential conversion feature limits the speed of the single channel SAR with 10b resolution at 320 MS/s [3] in the advanced technology node of 20 nm CMOS. Its conversion rate can be boosted either by using multibit-precycle [4], [5] or time-interleaved (TI) schemes [6], [7]. However, the SAR architecture demands a stringent noise requirement for the comparator design while aiming for high resolution. The signal-to-noise ratio (SNR) is usually dominated by the comparator's thermal noise. Further, the mismatch spurs due to the timing, offset and gain limit both signal-to-noise distortion ratio (SNDR) and spurious-free dynamic range (SFDR). All these nonidealities induce critical design challenges that limit the resolution of pure TI-SAR ADCs < 9b [6], [7]. The pipelined-SAR ADCs [8]–[12] still maintain their superiority in power efficiency with high resolution in deep submicron technology. The implementation of low stage gain (G) relaxes the desired noise requirement in the comparator and balances the tradeoff between the power dissipation and the gain-bandwidth product (GBW) requirement of the Op-Amp. Also, since a less number of Op-Amps is required, hence its power dissipation is no longer dominating, typically occupying around 20% of the total power consumption of the ADCs [11], [12]. As the first-stage SAR ADC quantizes a larger number of bits, the residue for amplification is comparatively small. This results in a smaller output swing, thus offering better amplification linearity. Therefore, the pipelined-SAR architecture has the potential to achieve higher resolution [8]–[10]. To further boost up its conversion speed, some designs adopt the TI scheme [9], [11]–[13]. Also, the nonlinearities due to offset and gain mismatches can be fixed in digital domain [8]–[10]. Time skews on the other hand are tolerated by design constraint [11] or avoided through architecture optimizations [12].

This paper presents a three-way TI subranging pipelined-SAR architecture [13] that achieves > 400 MS/s sampling rate and > 9b ENOB at Nyquist while maintaining good power and area efficiency. Several techniques are employed to achieve this:

1) The proposed hybrid ADC architecture [13] with multiple shared elements among the TI channels optimizes the die area and reduces the mismatches due to time skews and finite gain error from the Op-Amp.
2) The offsets from the comparators and Op-amp are all corrected on-chip through multiple calibration schemes. Timing and gain mismatches are tolerated by the design constraint, such that digital outputs do not need to be postprocessed during the measurement.
3) To speed up the SAR loop dynamic logic is utilized, and the SAR controller with an error-decision-correction (EDC) logic is used to enhance the robustness of the design.

II. ADC Architecture

The overall ADC architecture [13] is depicted in Fig. 1, consisting of a three-way TI subranging pipelined-SAR ADC operating at 150 MS/s for an aggregate of 450 MS/s. The flash ADC exhibits good power efficiency at 2b–3b resolutions, while the SAR ADC consumes larger dynamic power at the most significant bits (MSBs) transitions [2]. To reduce the

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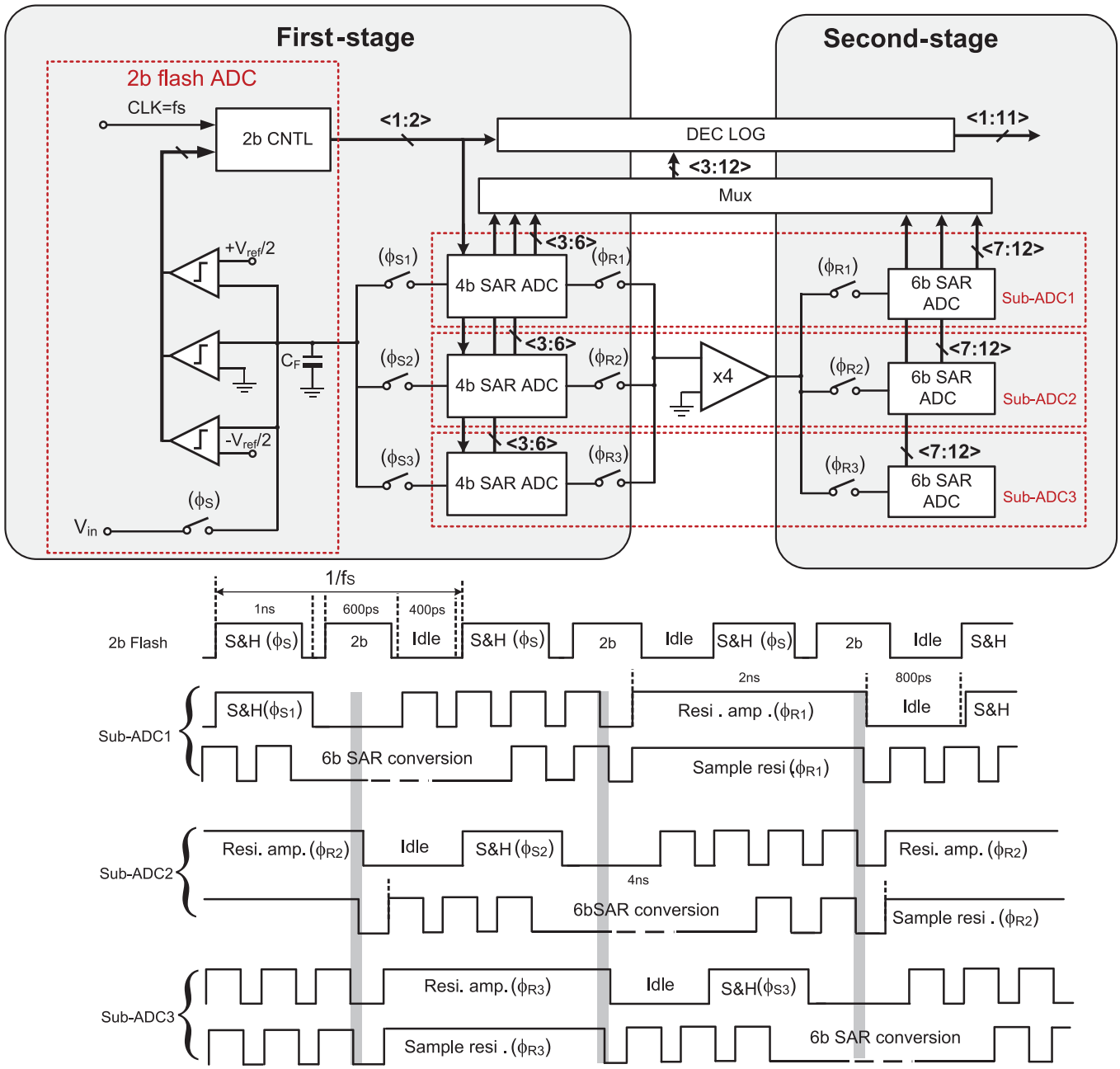


Fig. 1. Overall ADC architecture and its timing diagram.

number of transitions in leading bits that cause reference ripple, a 2b flash ADC with three-way TI pipelined-SAR architecture is proposed. The timing skews are avoided by series connection [14] of a master switch with the TI slave switches that synchronize the sampling time instances according to ϕ_S. The first- and the second-stages determine the coarse 6 bits and the fine 6 bits, respectively. One bit overlapping between two stages is designed for relaxing the sampling and comparison accuracies between the flash ADC and the TI sub-ADCs. The flash ADC resolves 2 leading bits, and the control logic passes the code to the corresponding sub-SAR ADC that resolves the remaining 4 bits. The residue is then amplified by 4 to the 6b SAR ADC in the second stage. The Op-Amp is shared by the sub-ADCs, and its bandwidth determines the optimum number of TI channels.

III. Mismatch Considerations

A. Subranging Mismatches

Since the first stage is implemented with a 6b flash +TI SAR architecture, the mismatch elements between the flash- and sub-SAR ADCs due to comparator offsets, reference voltages, and sampling networks cause conversion errors. With redundancy such errors within range can be tolerated in the subsequent bit cycles. Ideally, the residue (V_{resi}) should be within ± 0.5 least significant bits (LSBs). With one bit redundancy, the error tolerance region (ETR) goes up to $V_{\text{resi}} \pm 0.5$ LSBs. Once the errors are over ranging, they will remain as a final residue error. However, certain tolerance range can be occupied by noise. The total noise power of the ADC is mainly contributed from

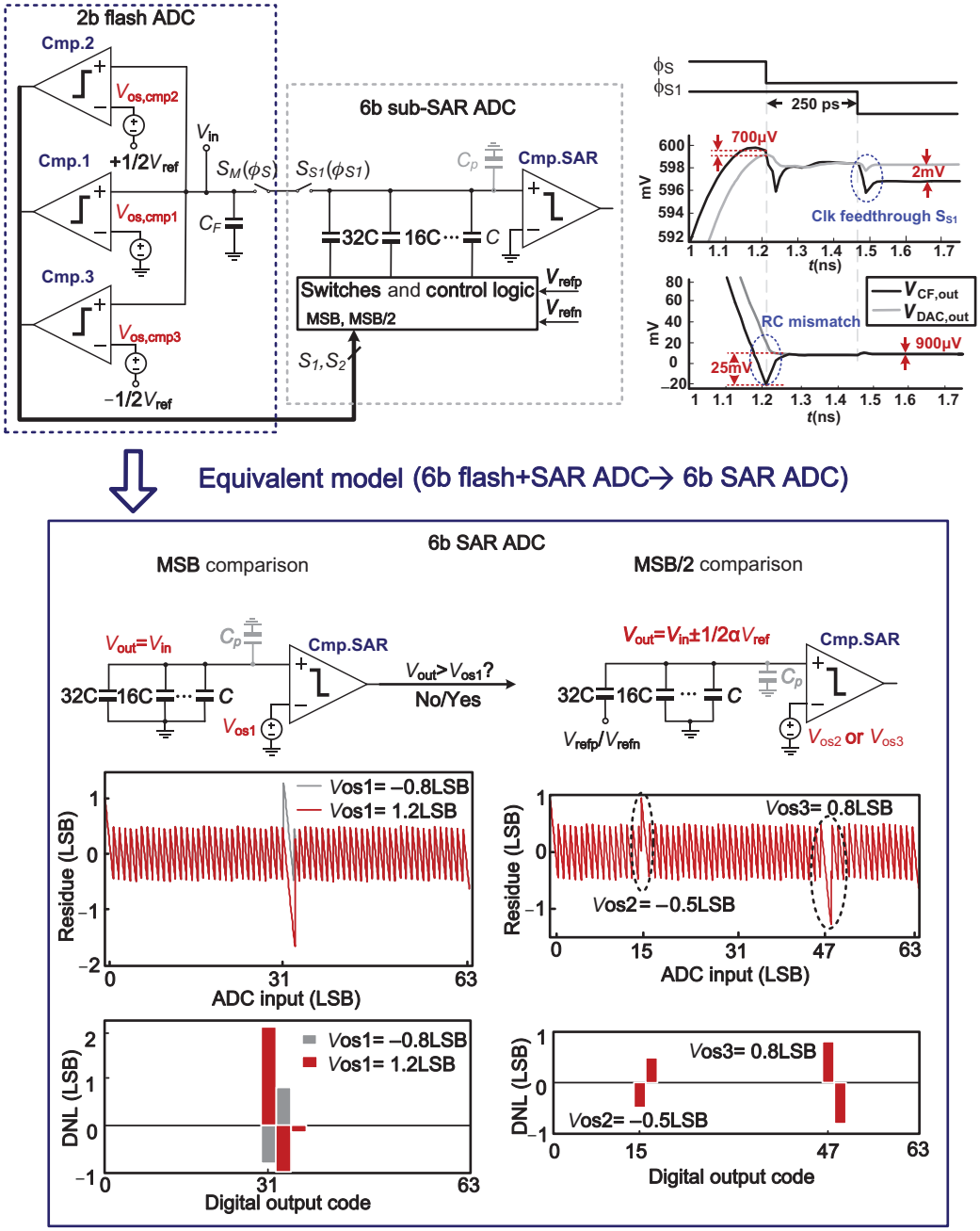


Fig. 2. 2b flash ADC + 4b subranging SAR architecture and its equivalent 6b SAR ADC model.

the quantization ($\frac{\Delta^2}{12}$) (where Δ represents the LSB), sampling (kT/C), and comparator ($V_{n,\mathrm{cmp}}^2$). As the sampling capacitor being over designed, it is ignored in the following discussion. When modeling the input referred noise voltage of the comparator as Gaussian random variables with a 3σ standard deviation of $\frac{\Delta}{2\sqrt{3}}$mV, the corresponding residue after 6 bit quantization would be $V_{\mathrm{resi}}\pm 0.25$ LSBs. The ETR is further reduced to ± 0.25 LSBs, and consequently, the conversion errors due to other circuit nonidealities should be suppressed within this range.

In the following, the residue error caused by the mismatch elements between the flash-SAR subranging architecture will be discussed. A 6b ADC built with 2b flash +4b sub-SAR structure is depicted in Fig. 2. As the input signal is sampled at the top-plate, the parasitic capacitance C_p causes an overall gain error of the reference voltage as αV_{ref}, which ultimately results in reference mismatches between flash and SAR conversions. To match the reference levels in the SAR ADC, two comparison thresholds in the flash ADC need to be adjusted to $\pm\alpha V_{\mathrm{ref}}/2$. Except the reference mismatch, the two-step subranging architecture also causes two types of mismatch: 1) the offset mismatches between the comparators and 2) the sampling mismatch. Fortunately, the above mismatches eventually result in comparison errors that can be corrected by redundancy.

The aforesaid subranging mismatches can be equivalent to a bit-dependent-offset error occurring during the SAR conversion, where the two-step operation is modeled in a 6b

SAR ADC, shown in Fig. 2. The input-referred offset voltages V_{os1}, V_{os2}, and V_{os3}, corresponding to the summation of mismatch errors, are injected into the SAR ADC's MSB and the MSB/2 comparisons, respectively. The MSB decision is reference-uncorrelated, which is determined directly by the comparison of two differential input signals, while it is impaired by the sampling and offset mismatches. The contributions for sampling mismatch ΔV_{in} originate from two sources. 1) Different RC time constants of the sampling networks, as the T/H capacitor C_F is much smaller than the DAC in the sub-SAR channel. 2) Clock feedthrough of the slave switch. For the first term, the mismatch is maximized at the middle of the input, where the slope of the signal is the highest (in Fig. 2). According to postlayout simulation, the maximum error is near ± 25 mV. However, as the slave switch S_{S1} is turned off 250 ps after the master switch S_M, it provides sufficient time for C_F and DAC to settle to the same value. For the second term, the mismatch is minimized at the middle and maximized at the two sides of the input. The subranging architecture is sensitive to the sampling mismatch near the MSB and MSB/2 transitions, where the mismatch in this design is $\approx \pm 90$ μV(± 0.01 LSBs) and ± 0.5 mV(± 0.05 LSBs), respectively. As the mismatch is quite small and well within the ETR, the clock feedthrough imposed on the subranging mismatch is not problematic. The ΔV_{in} associated with offset $V_{os,cmp1}$ in Cmp.1 is seen as an input referred offset $V_{os1}(V_{os1} = \Delta V_{in} + V_{os,cmp1})$ to the MSB comparison in the SAR ADC. As shown in Fig. 2, the offset causes the MSB's transition point to shift by V_{os1} leading to DNL errors at the MSB-1 (D31) and MSB (D32) digital outputs. As illustrated in Fig. 2, the $V_{os1} = -0.8$LSBs causes ± 0.8 LSBs DNL errors at D31 and D32, respectively. If V_{os1} further increases to 1.2 LSBs, it will cause a missing code at D32 and 2.2 LSBs DNL at D31.

The MSB/2 transition is reference-correlated, where the decision thresholds of the flash ADC are set by the reference voltages in Cmp.2 and Cmp.3. The conversion is also modeled as the MSB/2 transition in an SAR ADC. The MSB capacitor is charged/discharged to V_{refp}/V_{refn} according to the previous decision that generates the residue value of $V_{in} \pm 1/2\alpha V_{ref}$. It is compared with an input referred offset V_{os2} or V_{os3} at the negative side of the comparator. The V_{os2} and V_{os3} represent the summation of all the mismatch elements

$$V_{os2} = \Delta V_{in} + V_{os,cmp2} + 1/2V_{ref} - 1/2\alpha V_{ref} \quad (1)$$

$$V_{os3} = \Delta V_{in} + V_{os,cmp3} - 1/2V_{ref} + 1/2\alpha V_{ref}, \quad (2)$$

where $V_{os.cmp2}$ and $V_{os.cmp3}$ are the offset voltages in Cmp.2 and Cmp.3, respectively. The latter two terms represent the reference mismatch between flash and SAR ADCs. The mismatches are transferred to a bit-dependent offset causing DNL errors near MSB/4 and 3/4 MSB digital outputs.

The mismatches in flash + SAR subranging architecture cause only bit-dependent offset errors, which can be tolerated later by redundancy. However, considering the noise contribution mentioned previously, the total input referred offset voltages V_{os1-3} need to be suppressed below the ETR, i.e., ± 0.25 LSBs. Furthermore, this design relies on the comparators to detect and compensate the mismatches on-chip [15], the calibration accuracy is also limited by the comparator's noise. Therefore, the comparators in the first stage are designed with 3σ noise voltage of 0.18 LSBs (≈ 3.3 mV).

B. TI Mismatches in Sub-ADCs

The offsets in this design are contributed from the comparators in the sub-ADCs and the Op-Amp. Since the Op-Amp is shared by three channels and the redundancy relaxes the first-stage conversion accuracy, the total input referred offset requirement as previously discussed is $\pm 1/2^8 V_{ref}$. To achieve 68 dB SNDR with three TI-channels and stage gain of 4, the offset mismatch for the second-stage $\sigma_{\text{OM-2nd}}$ needs to be designed < 1.6 mV [16]. The gain mismatches among three channels come from the TI-MDACs and the second-stage DACs. The required gain mismatch between MDACs $\sigma_{\text{GM-MDAC}}$ and the second-stage DACs $\sigma_{\text{GM-2nd}}$ is $< 0.034\%$ and $< 0.14\%$, respectively [16]. In this design, the channel gain mismatch is tolerated by intrinsic capacitor matching and no gain calibration is employed.

Although the master–slave sampling network [13] is used to suppress the sampling mismatch from interleaving, there still exists sampling distortion and mismatches due to clock. The sampling distortion comes from the input-dependent timing skew of the master switch due to the use of top-plate sampling, whose gate voltage is charged to $V_{in} + V_{DD}$ during the sampling and then discharges by an RC network. Besides, the turn-off threshold voltage of the sampling switch is $V_{in} + V_{th}$. Therefore, the sampling instance would depend on the input signal. The simulated root mean squared (rms) value of such timing skew (Δt_{rms}) is ≈ 470 fs, which gives rise to the second harmonic and limits the total harmonic distortion (THD) to -64.3 dB in a single-ended sampling network. However, as the second harmonic can be suppressed by differential operation, it can be reduced to -103 dB.

Time spurs in the master–slave sampling network originates from the bandwidth mismatch as well as the signal-dependent feature when turning off the slave switches. The slave switches need to be smaller for reducing the signal feedthrough to the DAC. But, this will inevitably induce more bandwidth mismatch between the three interleaved sampling networks, thus leading to time spurs. Considering the design tradeoff, the master and slave switch is optimized to achieve a sufficient sampling bandwidth of 1.7 GHz as well as acceptable signal feedthrough with an NMOS device of $W/L = 7/0.06$ μm for the slave switch. Moreover, as the slave switch is turned off 250 ps later than the master switch, its V_{GS} would be $V_{in} + V_{DD} - V_{DAC}$ rather than V_{DD}, which potentially cause signal-dependent charge injection. Second, the clock feedthrough of the slave switch is also signal dependent since it turns off when its gate voltage being equal to $V_{DAC} + V_{th}$. However, these errors will not dominate the sampling THD, if the size of the slave switch is small. According to layout extraction, the C_{GD} of the slave switch is 0.7 fF, which is 0.08% of the total DAC capacitance. Finally, the signal-dependent leakage current of the slave switch is the main dominate source that causes time spurs. The top-plate of the DAC becomes a high impedance node when the master switch is turned off. The

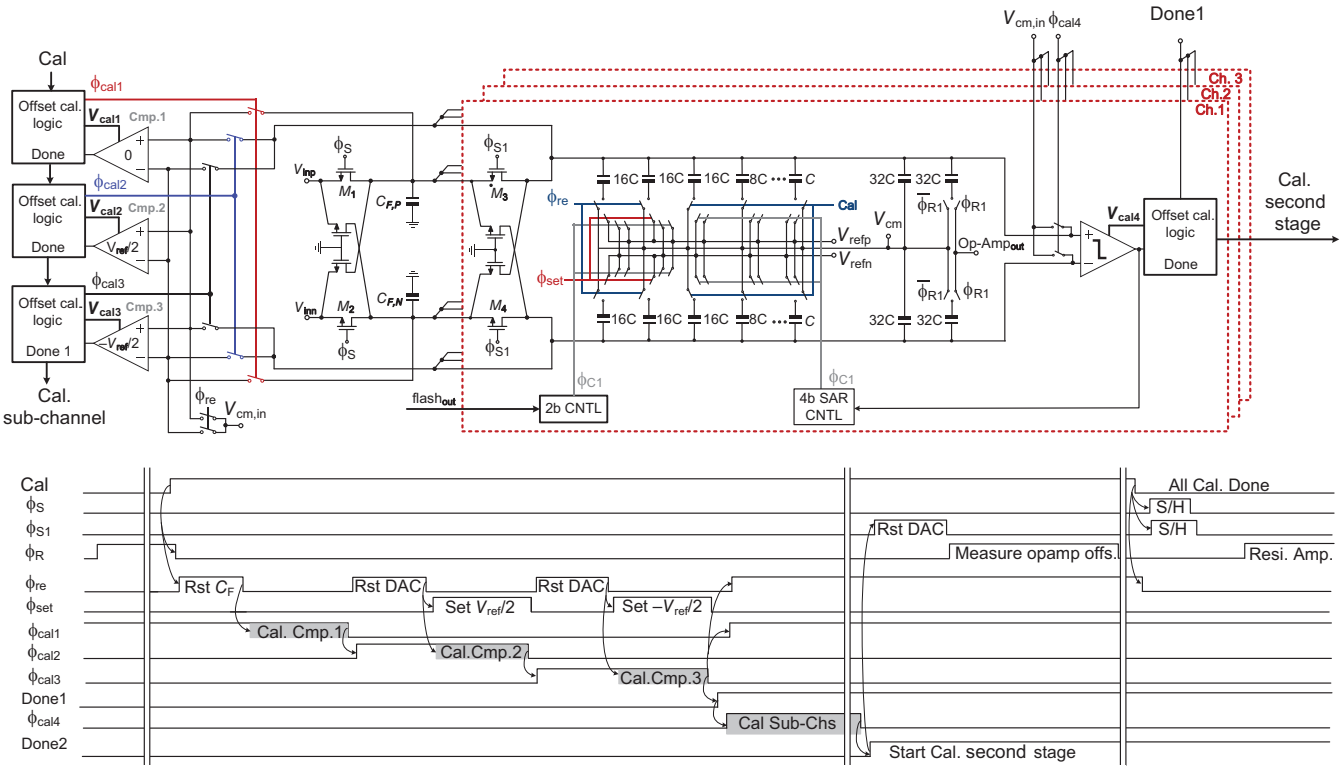


Fig. 3. Detailed circuit implementation of the first stage and offset calibrations for two stages together with its control timing diagram.

leakage current of the slave switch flows from its gate, whose voltage is $V_{\rm in} + V_{\rm DD}$ to its drain and the source. The effect becomes significant when there are time mismatches. However, the sensitivity and accuracy requirement for time mismatch in master–slave sampling network are much more relaxed than pure TI sampling front-end [6], [7]. According to simulation with the time mismatch $\sigma_{\rm TM}$ as large as 15 ps, the time spurs are still below -80 dB.

IV. Circuit Implementations

A. First-Stage ADC Design

The detailed implementation of the capacitive DAC is shown in Fig. 3, which consists of a 6b binary-weighted DAC array associated with 2×32C units. Two portions contain the same total unit of 64C for different functions. The 6b DAC performs binary-searched conversion, while the 2×32C units are kept connected to $V_{\rm cm}$ that serves as the capacitive dividing by 2 of the reference voltages. As the full-scale is 1.2 $V_{\rm p\text{-}p}$, the design uses three reference voltages $V_{\rm refp}$, $V_{\rm refn}$, and $V_{\rm cm}$, which are set to 1.2, 0, and 0.6 V, respectively. The feedback capacitor $C_{\rm FB}$ defines the stage gain of 4, as its value is 1/4 of the total array capacitance. The unit capacitance is 6.6 fF resulting in the total capacitance of 845 fF.

Other than the sampling kT/C and the device thermal noise, there are two main nonidealities impairing the SNDR of this ADC. First, the input signal feedthrough to C_F and sub-ADC, via the drain to source parasitic capacitances $C_{\rm DS}$ of the sampling switches, degrades the conversion accuracy. As shown

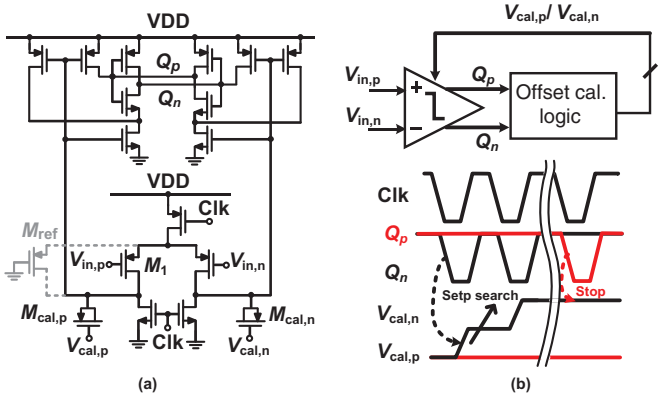


Fig. 4. (a) Schematic of comparator in the first stage w/ and w/o embedded reference. (b) Offset calibration and its control timing diagram.

in Fig. 3, the input signal is coupled to the top-plate of $C_{\rm F}$ through $C_{\rm DS}$ of the master switches (M1 and M2). The error causes only subranging mismatches, by using the cross-coupled dummy switches, the error is suppressed to ± 1.2 mV (0.13 LSBs of the first stage). However, the signal coupling via the capacitance of slave switches (M3 and M4) to the sub-SAR ADC would be more critical. When the channel 1 is sampling, channel 2 is performing the residue amplification. The signal coupled to the MDAC via the parasitic capacitance $C_{\rm DS}$ of slave switch in channel 1 degrades amplification accuracy, which needs to fulfill the overall ADC precision. Therefore, the signal feedthrough compensation to the slave switches in each sub-SAR ADC is also used to provide differential isolations. The

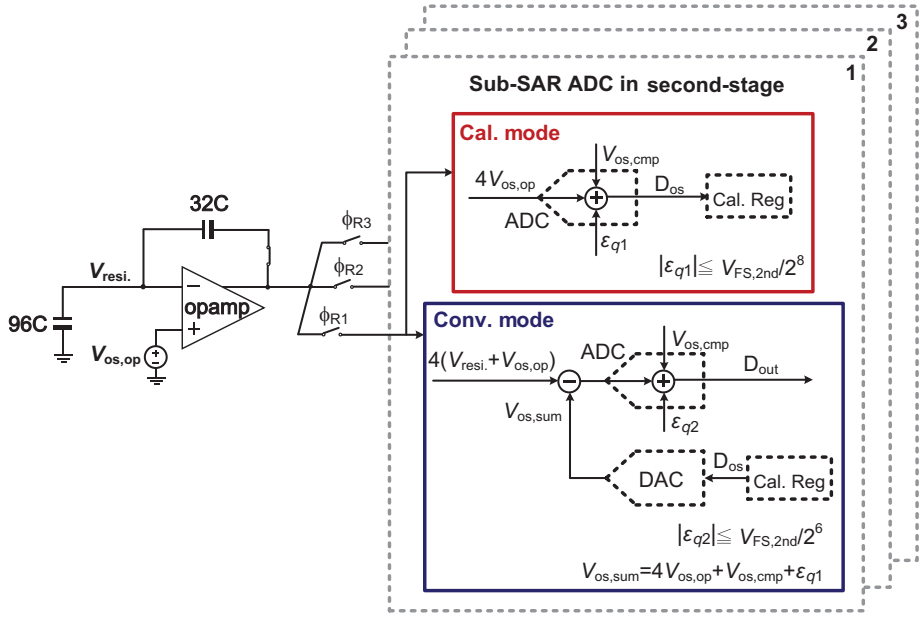


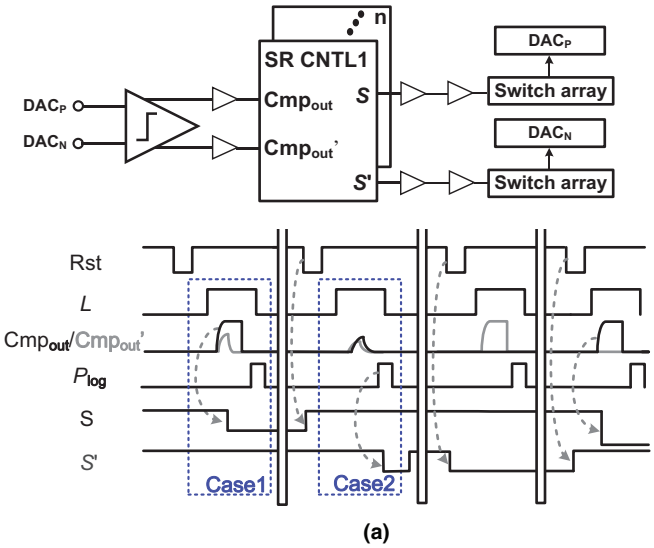
Fig. 5. Block diagram of the offset calibration in the second stage.

second limitation is the reference noise due to switching transients in the sub-SAR ADCs, while the pipelined-SAR architecture has a comparatively more relaxing accuracy requirement than the highly interleaved SAR ADC [15]. Benefiting from one bit redundancy and a $\times 4$ stage gain, the required accuracy of the reference voltages for the first- and the second-stage SAR conversion should be limited within $\pm V_{\rm ref}/2^7$ and $\pm V_{\rm ref}/2^{10}$, respectively. As mentioned before, the accuracy of the residue amplification is required to be the overall ADC precision. The reference interference among the TI channels will degrade the SNDR, as one of the sub-ADCs is amplifying the residue when the others are performing the conversion that cause reference ripples. One of the advantages in using this hybrid structure is the reduction in the number of switching transitions in the leading bits. From the timing diagram in Fig. 1, it can be observed that before the sub-ADC1 completes its amplification the first stage of the other sub-ADCs is either at the end of the SAR cycling or waiting for outputs from the flash side. The reference noise due to the switching transient is comparatively smaller.

B. Offset Calibrations

Two leading bits are determined by flash ADC that compares the input signal with the reference levels of 0 and $\pm 1/2V_{\rm ref}$. The decision thresholds are embedded [16] in the comparators. The offset calibration and its control timing diagram are shown in Fig. 3, where the calibration starts from the comparator (Cmp.1) in the flash side and corrects the offset error one-by-one. Once the calibration is enabled by a Cal signal, the sampling and amplification phases will be disabled immediately. As the Cmp.1 determines the MSB transition that is reference-uncorrelated, the comparator's input pair and the top-plate of $\rm C_{F,N}$ and $\rm C_{F,P}$ are reset to $V_{\rm cm,in}(400\ {\rm mV})(\Phi_{\rm re}=1)$. Next, the first comparison triggers the calibration logic to specify the offset polarity. As shown in Fig. 4 the comparator's outputs are then fed back continuously in a step-searched signal $V_{\rm cal,p}/V_{\rm cal,n}$ to the PMOS transistor $M_{\rm cal,p}/M_{\rm cal,n}$, which acts as a voltage-controlled capacitor and creates an unbalanced load to compensate the offset [16]. Note that the PMOS transistor $(M_{\rm ref})$ is implemented only in Cmp.2 and Cmp.3 for self-embedded reference, which will be presented later. The operation frequency of the calibration is synchronized to the internal SAR loop. Once the correction is completed a "Done" signal starts the calibration in the next comparator Cmp.2, which determines the $+V_{\rm ref}/2$ transition. The decision threshold in Cmp.2 is calibrated according to the MSB/2 reference level in the sub-SAR ADC. During the reset phase, both bottom- and top-plates of the DAC in the sub-SAR ADC as well as the inputs of the comparators are reset to their corresponding common-mode level. After this, the MSB capacitor in differential DAC is charged up to $V_{\rm refp}$ and $V_{\rm refn}$, respectively, which implies a $1/2\alpha V_{\rm ref}$ at its top-plate. As shown in Fig. 4, the threshold of Comp.2 is self-embedded at the input stage with a transistor $M_{\rm ref}$ [16], thus avoiding the resistive ladder for reference generation. The desired decision threshold is generated approximately via the $M_{\rm ref}$ with its gate connected to Gnd, as the threshold mismatch associated with offset mismatch will then be calibrated similarly as Comp.1. The $-1/2V_{\rm ref}$ transition in Cmp.3 is generated according to the signal path enabled by $\Phi_{\rm cal3}$, where a complementary reference level is properly applied for the calibration. Once the calibration in the flash ADC is completed, it starts the offset calibration in the sub-SAR ADCs.

The calibration scheme in the sub-SAR channels is much simpler, which is triggered one-by-one via the "Done1" signal from the previous stage. During the calibration, the capacitors $\rm C_F$, DAC, as well as the comparators' inputs are reset together to $V_{\rm cm,in}$ to sense offset voltage, which is then compensated similarly, as it was done in the previous comparators. A "Done2"



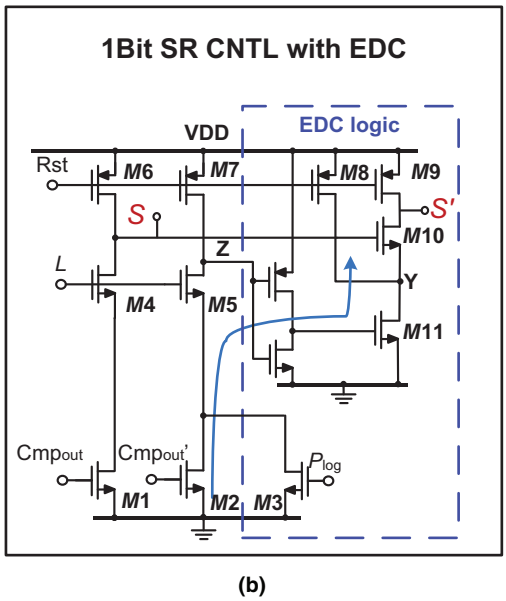


Fig. 6. (a) Signal processing and behavior from the comparator output node to the SAR controller. (b) Proposed SAR controller with EDC logic.

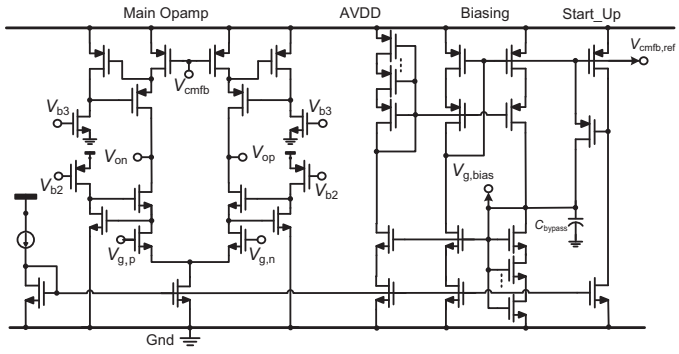


Fig. 7. Circuit schematic of Op-Amp.

signal that signs the completeness of the calibrations enables the sampling phase Φ_{S1} and the amplification phase Φ_R for the offset calibrations in the second stage.

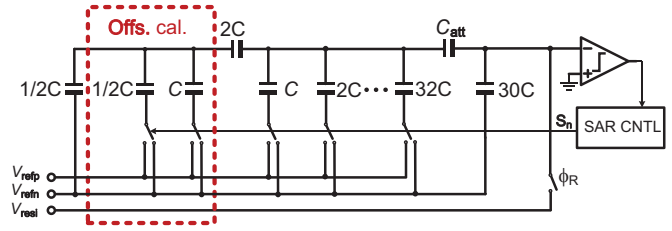


Fig. 8. Second-stage SAR ADC.

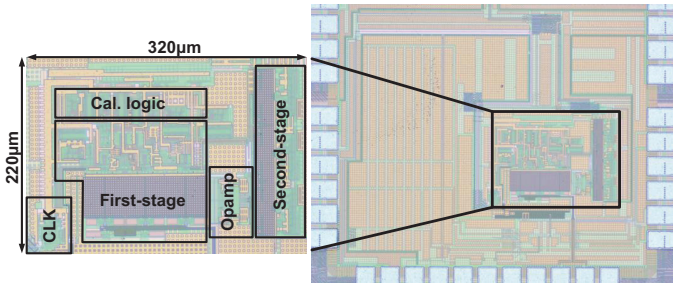


Fig. 9. Die microphotograph of the subranging pipelined-SAR ADC.

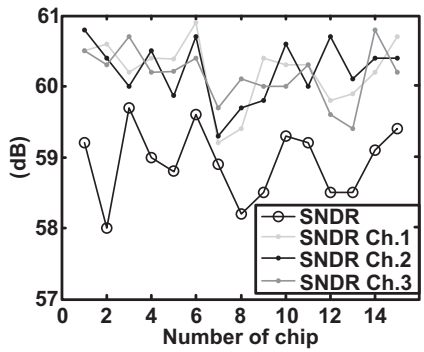


Fig. 10. Measured SNDR of total 15 chips at $f_{\rm in} = 10$ MS/s and $f_s = 450$ MS/s.

Next, the offsets from both Op-Amps and the second-stage comparators are corrected. To measure the offset, C_F and DAC are both reset during the sampling phase. Since the SAR conversion in the first stage is disabled ($V_{\rm resi.} = 0$), the signal amplified to the second stage is $4\times$ the Op-Amp's offset ($V_{\rm os,op}$) as illustrated in Fig. 5. This signal, associated with the comparator's offset $V_{\rm os,cmp}$ from the second stage, is then converted to a digital code $D_{\rm os}$ and stored in a calibration register (Cal. mode). The sub-ADC resolves 2 bits more during the calibration where $D_{\rm os}$ contains 8 bits. The solution suppresses the offset within 0.49 mV. It fulfills the offset requirement of the second stage that should be less than 1.6 mV. The operation repeats once in each sub-SAR channel and then the ADC resumes its normal conversion. The corresponding offset voltage measured in each channel will be subtracted during subsequent conversions.

C. SAR Controller With EDC Logic

The SAR controller stores the comparator's outputs and decodes them to the corresponding switch logic for the DAC. As shown in Fig. 6(a), two outputs of the comparator $\rm Cmp_{out}$

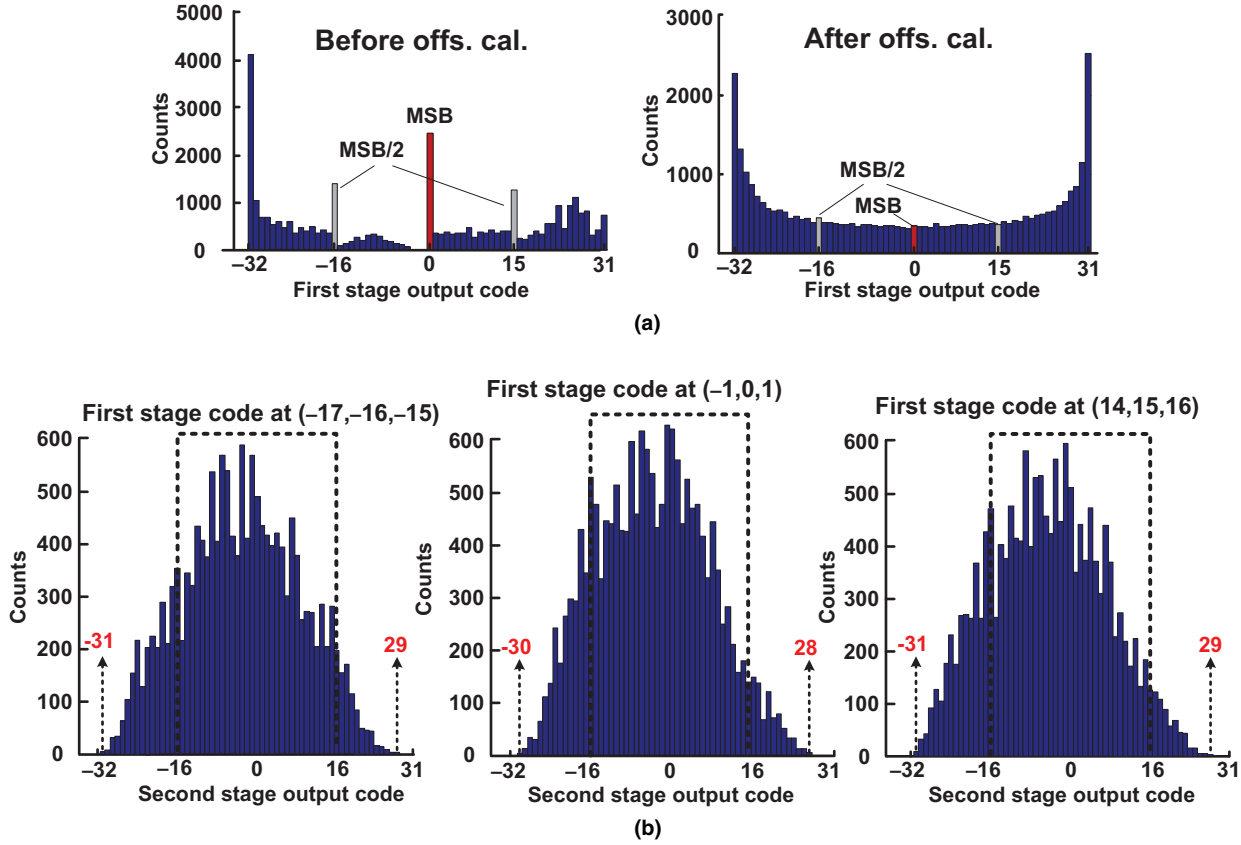


Fig. 11. Measured output code histograms. (a) Output code histogram of the first-stage 6b SAR ADC. (b) Output code histogram of the second-stage 6b SAR ADC at the signal near MSB and MSB/2 transitions.

and $\mathrm{Cmp_{out}}'$ are both applied to n-controller (CNTL) units. Both outputs remain low and complementary during the reset and comparison phase, respectively. The outputs of the CNTL S and S' signing the polarity of the switching logic are then buffered to control the DAC_P and DAC_N, respectively. According to the desired switching nature, S and S' should both be high initially and then remain complementary after the comparison. By observing the timing diagram of Fig. 6(a), two outputs (S', S) and the inner nodes (Z, Y) are at rest to "1" via signal Rst at the beginning. Ideally, once the transistors M4 and M5 are enabled by signal L, either output S or S' will be discharged to "0" according to the corresponding comparator's decision. As the circuit is fully dynamic, a protection scheme is required in the circuit to prevent the decision errors, which would guarantee that the final polarity of S and S' is complementary. The operation of the proposed EDC logic is depicted in Fig. 6(b). From case 1, if $\mathrm{Cmp_{out}}$ and $\mathrm{Cmp_{out}}'$ are both simultaneously high, S that is discharged to "0" before S′ will immediately turns off M10, which in turn disables the signal path in blue from $\mathrm{Cmp_{out}}'$ to the output S'. Therefore, S and S' are complementary after the comparison. In case 2, there exists metastability, where $\mathrm{Cmp_{out}}$ and $\mathrm{Cmp_{out}}'$ are too weak to reach the threshold voltage of M1 and M2. The ADC halts since no switching transient happens in this bit cycling. To prevent an error, a "$P_{\log}$" signal, which is generated by a constant delay after each comparison, is applied to each bit cycling. Therefore, the output of S' is finally pulled down to "0" via M3 once the "$P_{\log}$" goes high. However, there still exists the probability of logic processing error. If the $\mathrm{Cmp_{out}}$ reaches the threshold of M1 just after $\mathrm{Cmp_{out}}'$/"$P_{\log}$" signal goes high, both S and S′ go low. Since the logic output S and S' are not complementary, a conversion error happens. The worst measured bit error rate (BER) of the ADC is at 5.5E -7 with a few LSBs (< 10 LSBs) error magnitude.

D. Op-Amp Design

The Op-Amp is implemented with low-power considerations. The architecture of the Op-Amp [11] is shown in Fig. 7. It exploits the low output voltage swing (± 37.5 mV) using a telescopic topology with gain boost that enhances the gain. The used currents keep transistors in the subthreshold, which does not increase the headroom needed by the gain-boosted telescopic Op-Amp and makes it possible for a 1.2 V supply. The required dc gain is > 48 dB and GBW > 1.43 GHz. In this design, the Op-Amp achieves a low frequency gain of 66 dB gain, 2 GHz GBW (TT corner and 27 °C), consuming 1.2 mW power dissipation. The Op-Amp is biased by the process-tracked biasing network [11] that makes the Op-Amp insensitive to the supply, process, and reference current variations.

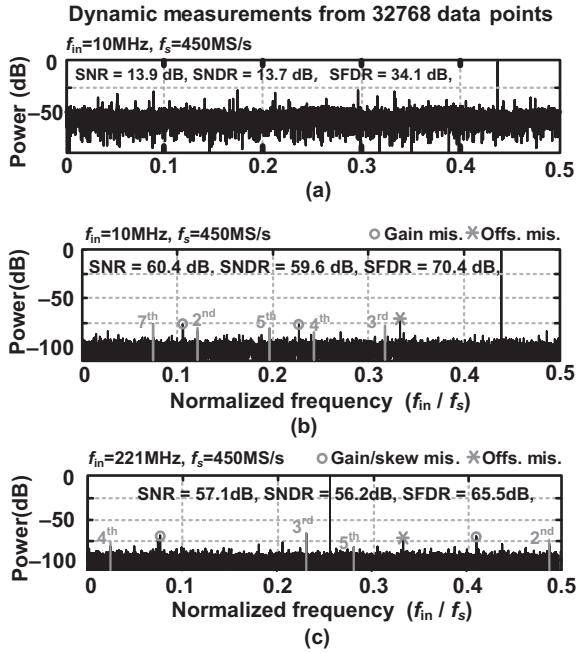


Fig. 12. Measured FFTs from 32 768 data output and decimated by 25. (a) Without offset calibration at $f_{\rm in} = 10$ MHz. (b) With offset calibrations at $f_{\rm in} = 10$ MHz. (c) With offset calibration at Nyquist input.

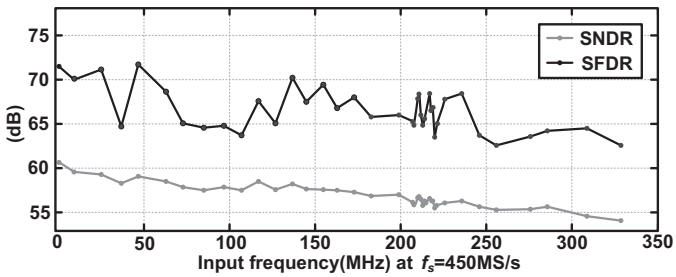


Fig. 13. Measured dynamic performance of SNDR versus $f_{\rm in}$.

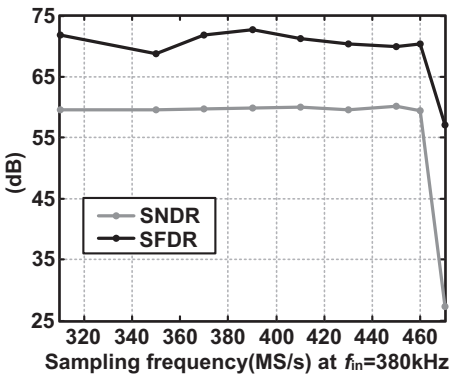


Fig. 14. Measured dynamic performance of SNDR versus f_s.

E. Second-Stage SAR ADC

The second-stage SAR ADC is conventional as shown in Fig. 8. It consists of an 8b DAC, a comparator [19], and a control logic. Two extra bits are enabled only during the offset calibration. With $\times 4$ stage gain, the second-stage SAR quantizing the residue from the first stage is 1/16 $V_{\rm ref}$. Besides,

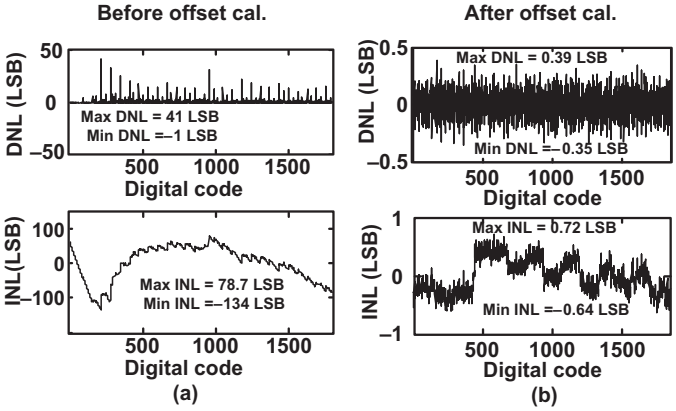


Fig. 15. Measured static performance. (a) Without offset calibrations. (b) With offset calibrations.

by 1b overlapping, the reference voltages for the second stage should be 637.5 and 562.5 mV, respectively. To avoid additional reference generation, the second-stage DAC utilizes a capacitive attenuator [11] to scale down the reference by 16. Therefore, two stages are implemented with the same reference voltages. One issue in the capacitive reference divider is that it induces a stage-gain error, which causes the spurs among the spectrum and degrades the SNDR. In this design, the problem was tolerated by intrinsic capacitor matching and careful layout routing. There is no gain-error calibration used here and the measured results shown in next section demonstrate that the stage-gain error does not impose main performance limitation.

V. Measurement Results

An 11 bit 450 MS/s subranging pipelined-SAR ADC was fabricated in a 1P7M 65 nm CMOS process and metal-oxide-metal (MOM) capacitors. Fig. 9 shows the die photograph of the design; the active area is 0.07 mm^2 (320 μm $\times$ 220 μm). The total power consumption is 7.4 mW at 1.2 V supply. The analog power consumption is 2.5 mW, including T/H, DAC, comparators, and Op-Amp, and the digital power consumption, including clock generator, SAR logic, and calibrations is 4.9 mW. The input and reference buffers are not implemented in this design. The reference voltages are generated externally, and a 300 pF on-chip decoupling capacitor is placed consuming an area of 0.028 mm^2.

The offset calibrations introduced in Section IV-B are all implemented on-chip. Fig. 10 illustrates the measured performance of total 15 chips at 10 MHz input and 450 MS/s sampling rate. The achieved average SNDR of the ADC and each subchannel is 58.9 and 60.2 dB, respectively, where the mismatch elements among the subchannels degrade the SNDR by 1.3 dB.

To measure the conversion error due to subranging mismatches, Fig. 11 shows the histogram of the output code at the first stage and the second stage (near MSB and MSB/2 transitions), respectively. For the first stage, the code is bounded at $+31/-32$, therefore, the MSB and MSB/2 transitions happen at codes 0, 15, and -16. Fig. 11(a) plots the code distribution

TABLE I
COMPARISON TO STATE-OF-THE-ART WORKS

	[8] CICC' 14	[9] VLSI' 14	[10] VLSI' 14	This work
Architecture	Pipelined-SAR	Pipelined-SAR	Pipelined-SAR	Pipelined-SAR
Technology (nm)	65	65	40	65
Resolution (bit)	13	12	12	11
No. of channels	1	2	1	3
Sampling rate(MS/s)	160	210	160	450
Supply voltage(V)	1/1.2	1	1.1	1.2
Input swing($V_{p\text{-}p}$)	1.2	1.6	2	1.2
SNDR at dc (dB)	68.3	63.5	65.3	60.8 (peak)
SNDR at Nyq. (dB)	66.2	60.1	66.5	56.2
DNL/INL (LSB)	N/A	0.7/1.5	N/A	0.4/0.7
Area (mm^2)	0.09	0.48	0.042	0.07
Power (mW)	11.1	5.3	5	7.4
FoM at DC (fJ/conv.step)	32.6	20.5	17.7	21
FoM at Nyq. (fJ/conv.step)	41.6	30.5	20.7	32
Calibration (on-chip)	No	No	No	Yes

of the first stage before and after the offset calibration. Before calibration, the subranging mismatches lead to large conversion errors at MSB and MBS/2 transitions, which are suppressed to sufficiently low after calibration. The codes histograms of the second stage are plot at the signal near MSB, MSB/2, and their ± 1 transition points in Fig. 11(b). Once there exist conversion errors and they are not over-range, the code should be bounded within $+31/-32$. The plot is within the full scale, which implies the conversion errors occurring previously are within the ETR.

The measured fast Fourier transforms (FFTs) at 10 MHz input frequency before and after offset calibrations are shown in Fig. 12(a) and (b), respectively. The offset mismatches at the first stage cause a large residue error. After offset calibrations, the ADC resumes to its normal operation, achieving SNDR of 59.6 dB and SFDR of 70.4 dB. Fig. 12(c) plots the FFT at Nyquist input, where the SNDR drops by 3.4 dB. The offset mismatch dominates SFDR at dc input, as the offset calibrations run at foreground by only once. The noise could potentially affect its accuracy. The offset spurs can be further suppressed by an averaging solution, but it is not implemented in this design. The spurs due to gain mismatch are below -75 dBFS. At Nyquist input the third harmonic dominates the SFDR and the spur due to time mismatch for the TI slave switch is -67 dBFS. Figs. 13 and 14 plot the swapping of both input and sampling frequency, respectively. The ADC achieves a peak SNDR of 60.8 dB at 380 KHz input with 450 MS/s sampling rate. The static performances before and after offset calibrations are shown in Fig. 15. Before offset calibration, the digital output contains large DNL and integral nonlinearity (INL), as the second-stage SAR operation is fully saturated by the offsets from the first-stage comparators and the Op-Amp. Once the offset calibration is active, the DNL and INL is compensated within 0.39 and 0.72 LSBs, respectively. The performance summary and comparison with State-of-the-art ADCs are shown in Table I. The design implements all the calibrations on-chip and achieves $> 2\times$ conversion speed than those reported in [8]–[10]. Also, considering that the full-scale of this design is well within the supply rail, the achieved conversion accuracy is still competitive with [9] and [10].

VI. CONCLUSION

This paper presented a 450 MS/s 11b subranging pipelined-SAR ADC in 65 nm CMOS. The proposed hybrid architecture avoids larger switching transients occurring in the residue amplification. This reduces the reference ripples and improves amplification accuracy. Moreover, the offset in each stage is properly corrected with low hardware cost allowing the ADC to achieve good conversion linearity without additional postprocessing error correction. Furthermore, the SAR ADC employs a dynamic SA controller with EDC logic to enhance design robustness.

REFERENCES

[1] C. C. Liu *et al.*, "A 10b 100-MS/s 1.13 mW SAR ADC with binary-scaled error compensation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC'10) Dig. Tech. Papers*, Feb. 2010, pp. 386–387.
[2] Y. Zhu *et al.*, "A 10-bit 100MS/s reference-free SAR ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, Jun. 2010.
[3] C. C. Liu *et al.*, "A 10-bit 320-MS/s low-cost SAR ADC for IEEE 802.11ac applications in 20-nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC'14)*, Nov. 2014, pp. 77–80.
[4] H. K. Hong *et al.*, "An 8.6 ENOB 900MS/s time-interleaved 2b/cycle SAR ADC with a 1b/cycle reconfiguration for resolution enhancement," in *IEEE Int. Solid-State Circuits Conf. (ISSCC'13) Dig. Tech. Papers*, Feb. 2013, pp. 470–472.
[5] C. H. Chan *et al.*, "A 3.8 mW 8b 1GS/s 2b/cycle interleaving SAR ADC with compact DAC structure," in *Proc. IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2012, pp. 86–87.

[6] N. L. Dortz *et al.*, "A 1.62GS/s time-interleaved SAR ADC with digital background mismatch calibration achieving interleaving spurs below 70 dBFS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC'14) Dig. Tech. Papers*, Feb. 2014, pp. 386–387.
[7] S. Lee *et al.*, "A 1GS/s 10b 18.9 mW time-interleaved SAR ADC with background timing-skew calibration," in *IEEE Int. Solid-State Circuits Conf. (ISSCC'14) Dig. Tech. Papers*, Feb. 2014, pp. 384–385.
[8] V. Tripathi and B. Murmann, "A 160 MS/s, 11.1 mW, single-channel pipelined SAR ADC with 68.3 dB SNDR," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC'14)*, Sep. 2014, pp. 1–4.
[9] C. Y. Lin and T. C. Lee, "A 12-bit 210-MS/s 5.3-mW pipelined-SAR ADC with a passive residue transfer technique," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014, pp. 1–2.
[10] Y. Zhou, B. W. Xu, and Y. Chiu, "A 12b 160MS/s synchronous two-step SAR ADC achieving 20.7fJ/step FoM with opportunistic digital background calibration," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014, pp. 1–2.
[11] Y. Zhu *et al.*, "A 50-fJ 10-b 160-MS/s pipelined-SAR ADC decoupled flip-around MDAC and self-embedded offset cancellation," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2614–2626, Nov. 2012.
[12] Y. Zhu *et al.*, "A 34fJ 10b 500 MS/s partial-interleaving pipelined SAR ADC," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2012, pp. 90–91.
[13] Y. Zhu *et al.*, "An 11b 900 MS/s time-interleaved sub-ranging pipelined-SAR ADC," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC'14)*, Sep. 2014, pp. 211–214.
[14] E. Janssen *et al.*, "An 11b 3.6GS/s time-interleaved SAR ADC in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC'13) Dig. Tech. Papers*, Feb. 2013, pp. 464–465.
[15] J. Zhong *et al.*, "Thermal and reference noise analysis of time-interleaving SAR and partial-interleaving pipelined-SAR ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2196–2206, Sep. 2015.
[16] C. H. Chan *et al.*, "A 5-bit 1.25-GS/s 4x-capacitive-folding flash ADC in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2154–2169, Sep. 2013.
[17] M. Gustavsson *et al.*, *CMOS Data Converters for Communications*. Norwell, MA, USA: Kluwer, 2000.
[18] G. Y. Huang *et al.*, "10-bit 30-MS/s SAR ADC using a switchback switching method," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 21, no. 2, pp. 584–588, Mar. 2012.
[19] C. H. Chan *et al.*, "A reconfigurable low-noise dynamic comparator with offset calibration in 90 nm CMOS," in Proc. *IEEE Asian Solid-State Circuits Conf. (A-SSCC'11)*, Nov. 2011, pp. 233–236.

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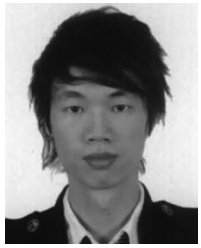

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