Nano-Watt Class Energy-Efficient Capacitive Sensor Interface With On-Chip Temperature Drift Compensation

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***Abstract*— This paper presents a nano-watt class energy-efficient capacitive sensor interface with on-chip temperature compensation. To achieve both high resolution and sensing accuracies, we exploit the fundamental limits of a two-step incremental-ADC and present a systematic study on the optimal coarse/fine bit allocations in the presence of mismatch errors. Efficient hardware reuse is ensured by utilizing the same loop filter, capacitive DAC, and digital controller in coarse/fine conversions for both capacitance and temperature readouts. A reconfigurable pre-gain stage for both capacitance and temperature sensing and a block-based data weighted averaging scheme are also employed to improve the overall system efficiency with 60% control overhead reduction. Optimized biasing circuit and subthreshold-biased amplifier with indirect compensation are utilized to achieve high accuracy with nano-watt power. Fabricated in a standard 0.18-μm CMOS process, the chip prototype consumes only 570 nW and achieves measured capacitance and temperature sensing inaccuracies of ±0.17 fF (1σ) from 0 to 10.8 pF and ±0.18 °C (3σ) from 0 to 100 °C, respectively. System level verification with a commercial MEMS pressure sensor shows a measured pressure sensing error improvement of >150× after temperature compensation.**

***Index Terms*— Capacitive sensor interface, energy efficiency, high accuracy, mismatch errors, pressure sensor, temperature compensation, two-step incremental-ADC, ultra-low power.**

I. Introduction

RECENT advances in both CMOS and MEMS technologies have created enormous opportunities in the emerging implantable and wearable wireless sensing applications [1]–[18]. With the advantages of zero static power consumption and good compatibility with CMOS circuitry, capacitive MEMS sensors which can access a wide variety of physical-quantities are well-suited in those power-/energy-constrained applications for collecting and analyzing the sensor data.

Table I summarizes the state-of-the-art MEMS-based capacitive pressure sensing systems to capture the trend and system requirements for wireless/implantable pressure sensing applications [1]–[14]. From Table I, it can be observed that such applications generally call for high sensing precision (e.g. sub-mmHg in pressure sensing), with a readout requirement of ~15b resolution and sub-fF precision. To achieve low cost miniaturized wireless sensing implementations, such systems are generally powered by micro-power solid-state batteries with high internal resistance or even passively powered without batteries, exhibiting stringent power/energy budget which calls for the continuous development of energy-efficient high accuracy sensor interface circuits with power consumptions down to the nW regime.

Various approaches for capacitive sensor interface designs have been investigated. The successive approximation register (SAR) topology [2], [3] is a promising candidate with ultra-low power (<160nW) and excellent energy efficiency (0.54 pJ/conv.-step) due to its intrinsic SAR operation, but with the achievable accuracy (>4.75 fF) limited by the mismatches in the capacitive DAC (CDAC). The SAR-based readout in [19] enhances the resolution to 1.1 fF with a hybrid coarse/fine CDAC, but the inverter-based amplifiers lead to high power consumption (>6 μW). By charging/discharging the base and input capacitors, both ultra-low power and high energy efficiency are demonstrated by the dual-slope topology in [7] through employing coarse/fine comparators. Yet, the achieved capacitance resolution of >8.7 fF is still limited by the comparator noise. For simple implementations, a highly digital capacitance-to-frequency readout for capacitive sensor can be implemented using a delay chain as demonstrated in [8], but with limited achievable resolution (>12.3 fF). To enhance the sensing resolution down to sub-fF, the capacitive readout based on the incremental ADC (I-ADC) [5], [20] and period modulation (PM) [13] through oversampling and noise shaping can be utilized. Nevertheless, the required high oversampling ratio (OSR) leads to excessive conversion cycles, ultimately penalizing their power and energy efficiencies. Even though mostly digital implementations can also be realized

Manuscript received January 7, 2018; accepted February 3, 2018. Date of publication February 7, 2018; date of current version March 9, 2018. This work was supported in part by the Macao Science and Technology Development Fund under Grant FDCT069/2016/A2 and in part by the Research Committee of University of Macau under Grant MYRG2015-AMSV-00140. The associate editor coordinating the review of this paper and approving it for publication was Dr. Zhichao Tan. *(Corresponding author: Man-Kay Law.)*

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Digital Object Identifier 10.1109/JSEN.2018.2803203

TABLE I
PERFORMANCE SUMMARY OF RECENT MEMS-BASED CAPACITIVE SENSOR INTERFACES

	Tech. (μm)	Area (mm^2)	Method	Input range (pF)	$T_{meas.}$ (ms)	Power (μW)	ENOB (Bits)	FoM_{cap} (pJ/c.s)	Cap. Res. (fF)	Temp. Calib.	MEMS Type	Application	MEMS Res. (mmHg)
[1]	0.18	0.1	SAR	0-16.14	0.04	3.84	11.8	45.8	4.5	No	Pressure	WSN	N/R
[2]	0.18	0.49	SAR	2.5-75.3	4	0.16	8.9-9.8	0.54-1.3	5.9	No	Pressure	WSN	0.4
[3]	0.18	5.7[&]	C/V+SAR	9.5	16.7	0.13	9.2	3.9	4.75	No	Pressure	Implantable	2.16
[4]	0.18	1.2	C/V+SAR	3.4-4.2	0.02	70	7.3	9.7	2.5	No	Pressure	WSN	N/R
[5]	0.18	0.2	I-ADC	0.5-3.5	1	80	14	4.8	0.05	No	Pressure	WSN	N/R
[6]	0.18	0.1	I-ADC	1.56[#]	200	7	7[#]	10.9	13	No	Pressure	Implantable	0.5
[7]	0.18	0.1	Dual-slope	5.3-30.7	6.4	0.11	7	5.3[*]	8.7	No	Pressure	Implantable	0.77
[8]	0.04	N/R	Delay Chain	$0.7\text{-}10^3$	0.019	1.84	8	0.14[^]	12.3	No	Pressure	WSN	1.39
[9]	0.13	0.07	Freq. Mod.	6-6.3	1	0.27	6.1	3.9	3.6	No	Pressure	WSN	N/R
[10]	0.18	0.46	SAR+I-ADC	0-24	0.23	33.7	15.4	0.18	0.16	No	Pressure	WSN	0.28
[11]	0.16	0.33	SAR+I-ADC	0-3.8	100	8.3	18.7	0.76	2.5×10^{-3}	Yes	Pressure	N/R	N/R
[12]	0.13	0.28[#]	Freq. Mod.	0-5.7	200	2.3	12	112	1.32	Yes	Pressure	Implantable	0.9
[13]	0.16	0.05	PM	0-8	0.21 (6.86)	14	10.6 (13.1)	1.87 (10.6)	1.4 (0.25)	No	Pressure	N/R	N/R
[14]	0.18	0.1	PM	6.4-9.8	17.5	18.4	10.4	238	2.05	Yes	Pressure	Implantable	1.46[#]

[*] One subrange FoM_{cap} [^] FoM_{cap} at 11.3 pF sensor capacitor [#] Extracted data from the literature
[&] Area of integrated MEMS included

by the frequency modulation readout as in [9] and [12] for ultra-low power, their energy efficiencies are limited due to the high OSR requirement (OSR=825 in [9]).

Recently, the two-step I-ADC topology [10], [11], [21] is becoming attractive due to its high energy efficiency improvement using coarse/fine converters while preserving the high resolution. In [11], the SAR+I-ADC architecture achieves both high resolution (∼2.5aF) and energy efficiency (0.79/pJ/conv.-step). Yet, the involved power-hungry integrators mandate a power consumption of 8.3 μW, and the issue on how coarse/fine bit can be systematically allocated is still lacking. While the work in [21] further improves the energy-efficiency (55fJ/conv.-step) by employing a VCO-based I-ADC for fine conversion with high resolution (∼1.1 fF), its power dissipation is significantly increased to 75 μW.

Based on the above discussion, it can be observed that existing works generally suffer from either limited energy efficiency for achieving a sub-fF sensing accuracy due to the suboptimal readout design or high power consumption in the order of μW which can be intolerable especially in many passively-powered systems. To address these challenges, this work presents a nano-watt class high accuracy capacitive MEMS pressure sensor interface with on-chip temperature drift compensation targeting for both energy- and power-constrained wireless pressure sensing systems. Apart from that, as the strong temperature dependencies of capacitive MEMS sensors [11], [22] can significantly degrade the sensing accuracy, on-chip temperature compensation is also utilized to ensure robust system operation in practical implementations. By reusing the same I-ADC for both capacitance and temperature sensing, both small system area and power/energy efficiencies can be achieved. A reconfigurable pre-gain stage for both capacitance and temperature sensing using the same CDAC and a block-based data weighted averaging (BDWA) scheme are also implemented to improve the overall system efficiency with reduced control overhead. A systematic study on two-step I-ADC is also introduced to evaluate its performance limits in the presence of mismatch errors to achieve optimal coarse/fine bit allocations for improved energy efficiency under a sub-fF capacitance resolution requirement. The power of the biasing and BJT-core for on-chip temperature sensing are optimized to achieve the target resolution with nA current consumption. Also, unlike the popular inverter-based integrator which draws significant instantaneous current that would overload the supply voltage in power-/energy-limited and/or passive systems, a subthreshold biased two-stage amplifier based on the indirect compensation technique in [23] is developed to achieve robust nW operation by significantly reducing the output stage power. The chip prototype fabricated in a standard 0.18-μm CMOS successfully achieves both ultra-low power consumption (570 nW) and high sensing resolution (14.1 bits). The achieved capacitance and temperature sensing are $\pm$0.17 fF (1σ) from 0 to 10.8 pF and $\pm$0.18°C (3σ) from 0 to 100°C, respectively. Together with the estimated power of the digital controller, the proposed system achieves figure-of-merits (FoMs) of 1.3 pJ/conv.-step (FoM_{cap}) in capacitance sensing, and 46 pJ°C^2 for resolution (FoM_{res}) and 3.7 nJ%^{2} for accuracy (FoM_{acc}) in temperature sensing, respectively. Measurement results together with a commercially available MEMS pressure sensor also demonstrate a reduced pressure sensing error by $>150\times$ after temperature compensation.

This paper is organized as follows. Section II outlines the proposed capacitive sensor interface with two-step I-ADC and addresses the fundamental limitations. Section III shows the circuit implementation details. Section IV summarizes the measurement setup and results. Finally, the conclusion is drawn in Section V.

II. PROPOSED CAPACITIVE SENSOR INTERFACE

Fig. 1 shows the proposed capacitive sensor interface with an on-chip BJT-based temperature sensor which shares the two-step I-ADC core and digital controller for recycling the same hardware resources based on two-step I-ADC conversions in both sensing modes. The multiplexed signal from the capacitive sensor C_S and the BJT-core ($V_{BE1,2}$) passes

through a reconfigurable pre-gain stage K, which can be adjusted by configuring the CDAC elements. Besides signal conversion, the total capacitance of CDAC (in the order of pF) also contributes to the reference capacitance C_{REF}, which is determined by the base capacitance of C_S and the capacitance sensing range. In the capacitance sensing mode, K is set to 1 so as to achieve an extended sensing range. However, the same K can result in under-utilization of the ADC's input range in the temperature sensing mode (e.g. ∼9% for a 1-V input range from 0∼100 °C by reading out the temperature dependent $\Delta V_{BE}/V_{BE}$ value), leading to an increased resolution requirement and reduced energy efficiency. Consequently, K is set to 4 in the temperature sensing mode to relax the DWA control complexity while increasing the ADC's input range to ∼36% without causing integrator saturation. Here, we take advantage of the large C_{REF} as required in the capacitance sensing mode to realize the pre-gain K as well as the two-step conversions with minimal overhead. The corresponding details will be outlined in section III-B.

A. Operations of Two-Step I-ADC

The recent two-step I-ADC architectures [24], [25] are advantageous in achieving both high energy efficiency and high resolution. Even though [25] realizes the extended accuracy by recycling the residual voltage from the coarse quantization to obtain an extra order of noise shaping, the involved residual computation will induce gain mismatches during conversion steps, sacrificing the linearity.

Similar to [24], this work employs a two-step I-ADC topology for coarse/fine conversions by dynamically converging the reference to an input range sub-band based on the coarse conversion result using identical integrators, comparators, and feedback CDAC for power/area reduction. A theoretical study on the performance limits of two-step I-ADCs and the issue of optimal coarse/fine bit allocations in the presence of mismatch errors lacking in existing two-step I-ADC topologies similar to [24] will also be presented in section II-B.

For the coarse conversion, the I-ADC operates for N_C cycles as in conventional second-order I-ADC to generate a bitstream bs which is further processed by the decimation filter. The obtained coarse result (D_C) controls the feedback signal to approach the input via the CDAC, effectively shrinking the quantization region by 2^{B_C} times, where B_C denotes the effective resolution of D_C. The two-step I-ADC then operates for N_F cycles with the identical I-ADC for the fine conversion to resolve the fine result (D_F) with an effective resolution of B_F. The combination of D_C and D_F contributes to the final output D_{OUT}. The decimation filter can be reused in both steps.

Theoretically, the signal-to-quantization-noise ratio (*SQNR*) depends on the loop filter order, the quantizer bits, and the number of cycles within one conversion period (N). A second-order loop filter with 1-bit quantizer is chosen to ensure good linearity. The resolution of the I-ADC can be calculated as

$$R_{tot} = \left\lfloor log_2\left(\frac{(N_C-1)\,N_C}{2}\right)\right\rfloor + log_2\left(\frac{(N_F-1)\,N_F}{2}\right), \tag{1}$$

where the total number of cycles N is the summation of N_C and N_F. To achieve the same *SQNR*, cycles N of the two-step I-ADC can be significantly reduced when compared to the conventional I-ADC (e.g. from ∼300 to ∼58 cycles at 92 dB). Here we choose $N_C = 12$ to resolve the 6-bit coarse resolution. Notice that in the case of such two-step I-ADCs, the total number of conversion cycles is generally dominated by the fine conversion. When the ADC is quantization-noise limited as in (1), an increase in N_C (and hence B_C) can reduce N_F for a certain R_{tot}. In practice, however, with the increase in the coarse bit B_C, the mismatches in the feedback CDAC can become apparent and dominate over the quantization noise.

B. DEM

In order to achieve the target accuracy in the feedback CDAC without degrading the overall resolution, data weighted averaging (DWA), which is a fast DEM method with first-order noise shaping, is chosen to suppress the mismatch errors. The CDAC element mismatch error is assumed to be Gaussian distributed. The noise power of the residual mismatch e_{MIS} after N_{DWA} averaging cycles is defined and bounded as

$$e_{MIS} = \left\{\frac{1}{N_{DWA}}\left|\sum_{i=1}^{N_{DWA}}\sigma_i\right|\right\}^2 < \frac{1}{N_{DWA}^2}N_e\sigma_{max}^2, \tag{2}$$

where σ_i is the relative error of the i-th capacitor, N_e is the number of CDAC elements to realize the required multi-bit feedback, and σ_{max} is the worst-case mismatch for all the capacitor, respectively. Notice that σ_{max} should be layout and process dependent. As in conventional DWA, the elements are sequentially selected with the pointer returning to the first set after the last set is utilized. From (2), it can be observed that a larger N_e requires more averaging cycles to achieve the same e_{MIS}. Fig. 2(a) plots the DWA averaging cycles N_{DWA} against N_e under different σ_{max}, with e_{MIS} set to −92 dB. It can be observed that the required averaging cycles apparently increases with N_e and σ_{max}. Fig. 2(b) plots e_{MIS} versus the DWA averaging cycles N_{DWA} for different N_e with σ_{max} set to 0.1%. As expected, e_{MIS} can be significantly suppressed with smaller N_e, and the required N_{DWA} to achieve a certain e_{MIS} ultimately set the lower bound of N_F.

Based on the observations in Fig. 2, e_{MIS} can be significant with large σ_{max} and N_e, and an increase in B_C may even result in an increased N, leading to poor energy efficiency. To quantify the effect of coarse/fine bit allocations towards the energy efficiency in two-step second-order I-ADCs, we study the residual mismatch noise e_{MIS} and the quantization noise (e_Q) as B_C varies based on the target resolution requirement (R_{tot}) and process matching parameter (σ_{max}). Here, we first assume that the ADC is not thermal noise limited. As both e_{MIS} and e_Q should satisfy the ADC overall accuracy constraint, the total conversion cycles N for different $N_e = 2^{B_C}$ is calculated as

$$N = \sqrt{2}^{log_2 N_e + 1} + \max\left\{2^{R_{tot}}\sqrt{N_e}\sigma_{max}, \sqrt{2}^{R_{tot} - log_2 N_e + 1}\right\}, \tag{3}$$

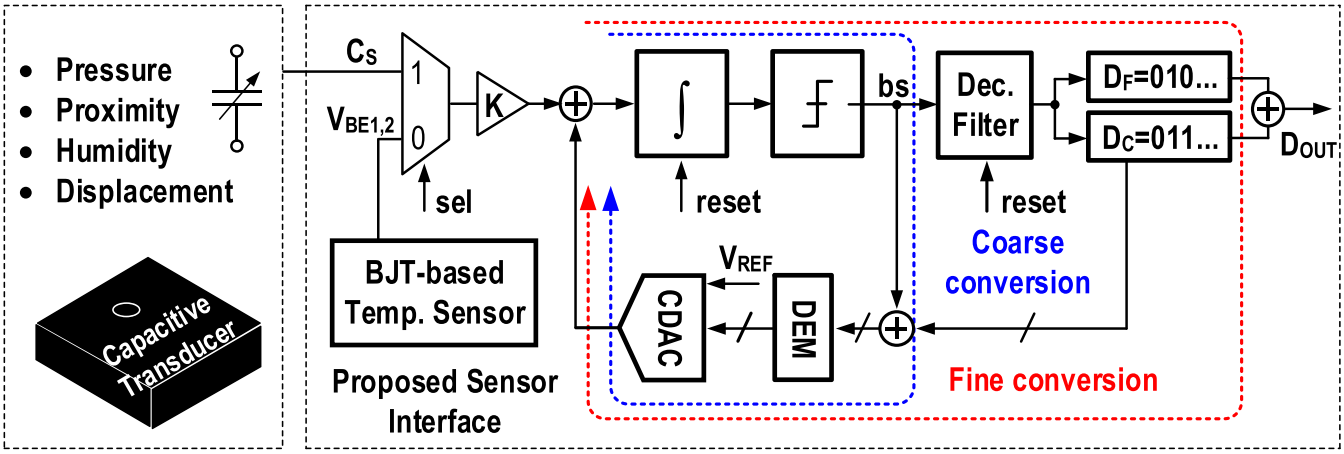


Fig. 1. System overview for capacitive sensor readout with the proposed sensor interface, where CDAC serves as the reference cap C_{REF}.

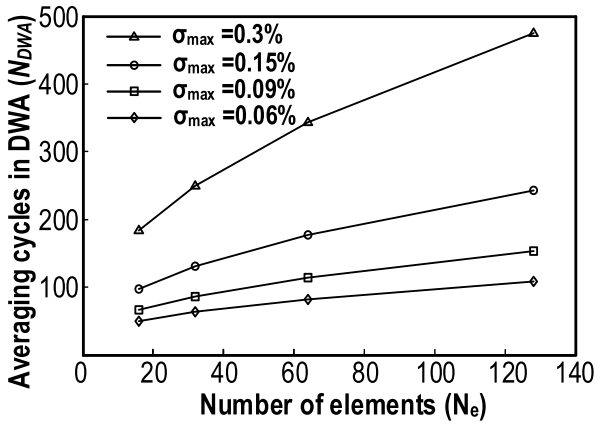


Fig. 2. (a) The DWA averaging cycles N_{DWA} against N_e for various σ_{max}, with $e_{MIS} = -92$dB. (b) e_{MIS} versus the DWA averaging cycles for different N_e with identical σ_{max} of 0.1 %.

where the first and second terms represent the required cycles in the coarse and fine conversions, respectively. Notice that the required cycles for a particular R_{tot} for both e_{MIS} (i.e. $2^{R_{tot}}\sqrt{N_e}\sigma_{max}$) and e_Q (i.e. $\sqrt{2}^{R_{tot}-log_2 N_e+1}$) depends on $N_e = 2^{B_C}$ with opposite trends. As a result, there exists an optimal B_C and B_F for a two-step I-ADC to achieve a certain resolution requirement and matching constraint. Fig. 3 studies the relationship between the total number of cycles N (i.e. N_C+N_F) and the achievable resolution R_{tot} for various B_C and B_F allocations under different σ_{max}. To attain the resolution R_{tot}, the total required N is indicated in solid lines when the resolution is limited by e_{MIS}, and in dashed lines when the resolution is limited by e_Q, respectively. The scaling coefficients of the integrators are set to 0.5 in this study. For a conventional second-order I-ADC (i.e. single-step), the cycles N is calculated as $\sqrt{2}^{(R_{tot}+1)}$, which is also included in Fig. 3 indicated by a solid bold line for comparison. The cross points of e_{MIS} and e_Q for various B_C are denoted with solid markers. For a small σ_{max}, enhancing the coarse resolution B_C is beneficial to achieve lower resolution. For instance, to achieve a 14b resolution with σ_{max} of 0.04%, N is only 40 for $B_C = 6$, but increased to 94 cycles for $B_C = 3$. Whereas, for a large σ_{max}, e_{MIS} can dominate over e_Q, and it is not beneficial to allocate more bits in B_C over the resolution range of interest (from 12 to 22 bits). For better illustration, Fig. 3(a-d) only plot those instances with cross points within the interested resolution range. In addition, when compared with single-step I-ADC, the two-step architecture exhibits advantages of reduced cycles for low resolution designs. While for higher resolution, the two-step I-ADC requires even more cycles and is inferior since the cycles for averaging mismatch error increase faster than that for quantization noise suppression. For instance, with a σ_{max} of 0.2%, the two-step architecture requires 2880 cycles to achieve a resolution of 20b with B_C of 4 bits, while the single-step one only demands 1850 cycles. Notice that the theoretical analysis for optimal coarse/fine bit-allocation can still be applied to similar architectures (e.g. [24]) with minimal modifications related to the evaluation of N_C.

C. Noise Sources

Apart from the mismatch error e_{MIS} and the quantization noise e_Q, the thermal noise (e_{TH}) should also be considered. This section outlines the noise performance of the proposed two-step I-ADC in both the coarse and fine conversions. With a quantization step Δ, we consider e_Q to be uniformly

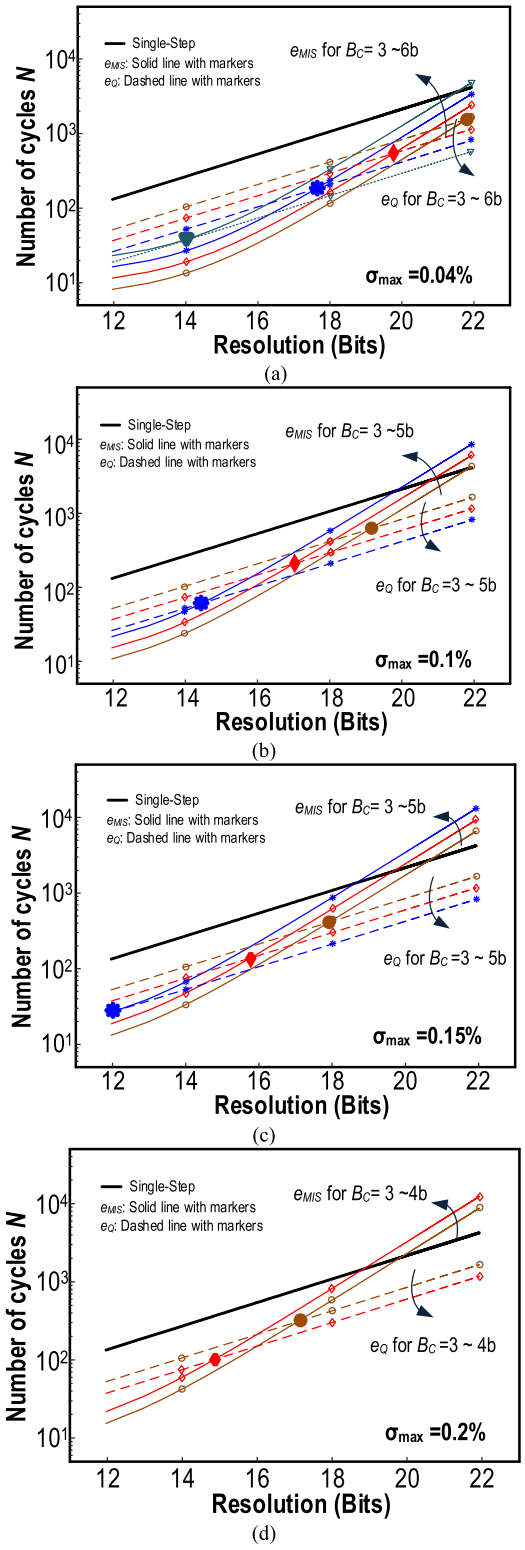


Fig. 3. The total number of cycles N versus the achievable resolution for various B_C and B_F allocations, regarding DWA errors (solid lines) and quantization noise (dashed lines) for (a) $\sigma_{max} = 0.04\%$; (b) $\sigma_{max} = 0.1\%$; (c) $\sigma_{max} = 0.15\%$; and (d) $\sigma_{max} = 0.2\%$. The markers indicate the crossover points of e_{MIS} and e_Q under different B_C. The solid bold lines represent the single-step I-ADC for comparison.

distributed in the range of $[-\Delta/2, \Delta/2]$ and zero otherwise, resulting in a noise power of $\Delta^2/12$. Therefore, e_Q decreases by a factor of 4 with every additional bit. The input-referred e_{TH} is determined by $4kT/(N \cdot C_{REF})$ for N cycles. The target is to achieve the required resolution under the constraints of each noise source with the minimum number of conversion cycles N. In general, e_Q is the dominant noise source during the coarse conversion and can be reduced by increasing the coarse conversion cycle N_C, while all the three noise sources should be considered during fine conversion. Thus, we investigate the relationships between the noise contributions and fine conversion cycles N_F as follows.

Here, we consider the design of a 15b two-step second-order I-ADC and obtain the optimal conversion cycles, taking into account for all the noise sources e_{TH}, e_{MIS} and e_Q. Fig. 4 plots e_{TH}, e_{MIS} and e_Q versus N_F for $N_e = 16$, 32, 64 and 128 (corresponding to $B_C = 4$, 5, 6, and 7). The unit capacitance (C_u) and the worst-case mismatch σ_{max}, which are both process dependent parameters, are set to 44 fF with a minimum-sized 5×5 μm^2 MIM capacitor and 0.1% (1σ) based on the device characterization report for the chosen 0.18-μm CMOS process, respectively. From Fig. 4 (a-d), we can observe that with an increase of N_e (and hence C_{REF} and B_C), e_{TH} and e_Q reduces accordingly, whereas e_{MIS} increases as in (2). It should be noted that the noise power from e_{TH}, e_{MIS}, and e_Q are inversely proportional to N_F, N_F^2 and N_F^4, respectively. With practical N_e, e_{MIS} is larger than e_{TH} when N_F is small, and e_{TH} will dominate over the other noise sources with a sufficiently large N_F. There exists a particular N_F where e_{TH} and e_{MIS} meet, and can be expressed as

$$N_F = \frac{N_e^2 \cdot \sigma_{max}^2 \cdot C_u}{4KT}. \tag{4}$$

From (4), it can be observed that different N_F can be obtained with various N_e. However, the obtained value should fulfill two main design requirements: 1) satisfy the noise floor defined by the target resolution; and 2) above the in-band e_Q by $\sim$10 dB [26]. We assume that the noise floor requirement is -92 dB. As shown in Fig. 4 (a-d), we can observe that $N_e = 32$ is the optimum choice in this setting with minimum N_F, where N_F is roughly 60 to fulfill the -92 dB requirement and $e_Q$is around 7 dB lower than e_{TH}. For $N_e = 16$, the in-band e_Q dominates over the other noise sources until $N_F > 70$. For $N_e = 64$ or 128, e_{MIS} dominates the other two noise sources, and the obtained N_F is as large as 240 and 480, respectively.

D. Number of Conversion Cycles

Based on the above noise analysis, to achieve an overall 15-bit resolution with minimum number of cycles, the coarse resolution B_C should be 5 bits and the remaining 10 bits should be realized in fine conversion. To obtain a wide non-overloaded range, the coefficient of the integrators should be chosen properly and cannot be set independently since it can affect the loop stability. In this work, we employ a feed-forward I-ADC to lower the integrator's swing. Similar to [27], by simulating using the integrators maximum allowable input, the coefficients for the first and second integrators can be found to be 0.7 and 0.8, respectively. With these coefficients, 6 bits within 16 cycles can be achieved in coarse conversion (with 1 extra bit to serve as guard band to prevent the risk of

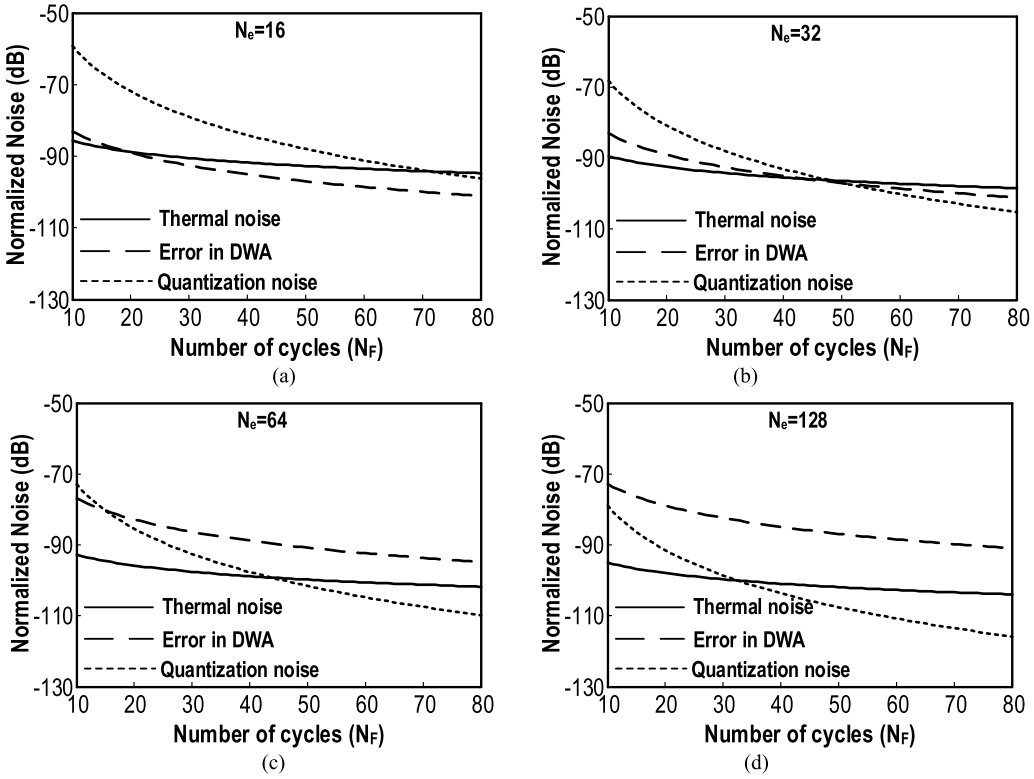


Fig. 4. Noise sources (thermal noise, mismatching error, and quantization noise) in fine conversion for different N_e.

reference misalignment). Correspondingly, N_F is set to ~70 to resolve the 10-bit B_F.

III. Circuit Implementations

This section describes the circuit implementation and the front-end configuration of the proposed capacitive sensor readout. The biasing circuit and the BJT-core are firstly introduced, followed by the front-end design and DWA control methodology for both the temperature and capacitance sensing modes. In this work, the capacitive MEMS sensor E1.3N [28] is chosen as a design example. It exhibits a sensor base capacitance of ~6 pF. In order to achieve a pressure resolution of 0.3 mmHg (similar to [6], [7], [10], and [12]), the targeting capacitance resolution is around ~0.3 fF, corresponding to a resolution requirement of ~14 bits. This sensor also shows a measured worst-case temperature coefficient of 0.8 fF/°C, and a temperature sensing accuracy of ~0.2 °C is required to effectively compensate the capacitance sensing error to be within 0.5 LSB. With reference to commercial products targeting on similar applications (e.g. wearable sensing and/or pressure/humidity monitoring applications in [29] and [30]), the temperature compensation range is set to 0 to 100 °C in this design.

A. Biasing Circuit and BJT-Core

The BJT-core with biasing circuit for temperature sensing is shown in Fig. 5. It consists of two identical substrate-PNPs Q_1 and Q_2 biased at a $1{:}p$ current ratio. The base-emitter voltage V_{BE1} (V_{BE2}) of $Q_1(Q_2)$ is complementary-to-absolute-temperature ($CTAT$), while the voltage difference $\Delta V_{BE} = V_{BE1} - V_{BE2}$ is proportional-to-absolute-temperature (*PTAT*). A reference voltage can then be generated as $V_{REF} = V_{BE2} + \alpha \cdot \Delta V_{BE}$, where α is the gain factor to compensate for the temperature coefficient of V_{BE2} (≈ -2 mV/°C) and ΔV_{BE} (≈ 0.14 mV/°C for $p = 5$). The exact value of α can be obtained from simulations for a particular BJT device and biasing condition. In [31], the ratio $V_{BE}/\Delta V_{BE}$ which contains the temperature information is first extracted, followed by α calibration to map the nonlinear output to the digital ratio μ using post-linearization. In this work, we utilize the output ratio $X = K\Delta V_{BE}/V_{BE}$ for temperature measurement so as to relax the required ADC resolution, and better match the multi-sensor readout requirements by incorporating the pre-gain K for power saving. Even though a higher K can reduce the corresponding resolution requirement of the ADC, it can also increase the risk of overloading the integrator. Hence, we choose $K = 4$ to balance the ADC dynamic range and the system reliability over mismatch and process spreads. The ratiometric readout (μ) is defined as

$$\mu = \frac{\alpha \Delta V_{BE}}{V_{BE} + \alpha \Delta V_{BE}} = \frac{\alpha' X}{1 + \alpha' X}, \tag{5}$$

where $\alpha' = \alpha/K$ is the gain incorporated in the digital domain. μ is then translated to degree Celsius by using $D_{out} = A \cdot \mu + B$, where $A \approx 600$ and $B \approx -273$ are the calibration parameters [32].

In the bias circuit, a *PTAT* current I_{bias} incorporated with β-compensation was chosen to bias Q_1 and Q_2 in the core to partially cancel the V_{BE} curvature and enhance the linearity and sensing accuracy [32], [33]. In terms of the biasing core,

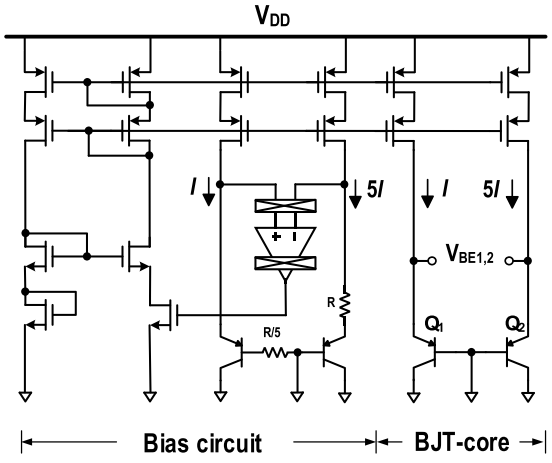


Fig. 5. Schematic of bias circuit and BJT-core for temperature sensing (DEM of current source in BJT-core omitted for clarity).

a small BJT biasing current can increase the spread of V_{BE} and ΔV_{BE} due to the increased non-linearity in the BJT current gain β. For biasing the BJT core using nA current, both the small β ($\sim$2 for the PNP BJT in the chosen 0.18-μm CMOS process) and its temperature dependency can induce error in V_{BE} and ΔV_{BE} as follows:

$$V_{BE} = \frac{kT}{q}\left[\ln\left(\frac{I_{bias}}{I_s}\right) + ln\left(\frac{\beta_2}{\beta_2+1}\right)\right], \quad (6)$$

$$\Delta V_{BE} = \frac{kT}{q}\left[\ln(p) + \ln\left(\frac{\beta_1}{\beta_2}\cdot\frac{\beta_2+1}{\beta_1+1}\right)\right]. \quad (7)$$

From (6) and (7), it can be observed that β can result in gain errors, while its temperature dependence can lead to residual curvatures. Both error sources cannot be directly trimmed out using one-point calibration. Based on the extracted β (T) from simulation, we target for an error tolerance of $\pm$0.05 °C in order to achieve the target accuracy of $\pm$0.2 °C. Consequently, I_{bias} is set to 17 nA. In addition, the biasing current in the BJT-core and the current mirror matching in nA-level becomes worse. To suppress the mismatch in the current sources, cascoding current mirrors (Fig. 5) with DEM and common-centroid layout are utilized to achieve a matching accuracy of 0.02%. In this design, the total front-end power is optimized to be 248 nW.

To meet the settling requirement, I_{bias} and the sampling capacitors in temperature sensing mode (C_{SMP}) are related by [34]

$$C_{max} \leq \frac{1}{2\cdot f_{clk}\frac{KT}{q}\cdot}\left[\frac{I_{bias}}{\ln\left(\frac{1}{\varepsilon}\right)}\right], \quad (8)$$

where C_{max} is the maximum value of C_{SMP}, f_{clk} is the sampling clock frequency and ε is the settling accuracy. For f_{clk} = 2 kHz, the corresponding C_{max} should be roughly 17.5 pF. For thermal noise considerations, we set the total in-band thermal noise, given by $4kT/(N\cdot C_{SMP})$ where N is the number of cycles in one temperature conversion, to the required quantization noise level of 8.8 μV_{rms}. Consequently, with N = 80 cycles, the minimum C_{SMP} can be estimated to be 2.7 pF. In this work, the total CDAC capacitance in fully differential mode is sized to be 14.08 pF with consideration of the pre-gain K, the capacitance sensing range and the CDAC feedback for fine conversion (i.e. N_e = 32). To sufficiently reuse the CDAC in temperature sensing mode, C_{SMP} for sampling V_{BE1} or/and V_{BE2} is set to $4\cdot C_{REF}$/5 so as to realize the 4: 1 ratio while satisfying the above settling and thermal noise requirements.

B. Front-End Configurations for Temperature/Capacitance Sensing

The operation principle of the two-step I-ADC for both the temperature and capacitance sensing modes is shown in Fig. 6. In this work, each CDAC element is implemented using a minimum-sized 5×5 μm^2 MIM capacitor of 44 fF available in the selected 0.18-μm CMOS process, with an estimated worst-case mismatch error of $\sim$0.1% (1σ) based on the device characterization report with overhead (e.g. mismatch in DEM switches, routing parasitic, gradient effects). As shown in Fig. 6(a), both the sampling and integration phases in the temperature sensing mode can be accomplished within one clock cycle, effectively doubling the conversion speed. In Φ_1, C (=32C_u) samples V_{BE2} while 4C simultaneously samples ΔV_{BE}, corresponding to a stored charge proportional to (4ΔV_{BE}-V_{BE2}). In Φ_2, the input is swapped and the total integrated charge becomes 2×(4ΔV_{BE}-V_{BE2}). According to the value of bs, C either samples V_{BE2} (bs=0) or is switched to ground (bs=1). After 16 cycles, the output bitstream is processed by the decimation filter to obtain the 5-bit D_C for fine conversion. In the fine conversion, DEM controls a total of *32* C_u to switch between ground and V_{BE2} according to D_C and bs, which is equivalent to quantizing the input signal $4\cdot\Delta V_{BE}$ within one of the input sub-bands of size V_{BE2}/32.

In capacitance sensing mode as shown in Fig. 6(b), the capacitive sensor C_S is connected directly to the I-ADC input. The I-ADC determines the ratio C_S/C_{REF}, where C_{REF} = 160 C_u is the on-chip reference capacitor. All the CDAC elements with a total capacitance of 14.08 pF in differential input are reused.

C. BDWA Control

To achieve K = 4 in temperature sensing mode with a 5-bit D_C feedback, a total of $2^5\times$ (4 + 1) = 160 C_u is required. This inevitably results in increased DEM control complexity. To resolve this issue, the block-based DWA (BDWA) method is employed for DEM control to meet the accuracy requirement while significantly reducing the implementation overhead [34]. The segmentation and control of the capacitors is described in Fig. 7. The 160 elements are divided into 24 sub-banks (each with 5C_u) and 40 unit elements so as to achieve the accurate 4:1 ratio in the temperature sensing mode and precise sub-ranging (with ratio of 32:1) during the fine conversions in both modes. The number of required control signals can be reduced by 60% when compared with the conventional DWA approach with individual control (from 160 to 64). Simulations results show that BDWA requires 52 cycles to achieve the 15-bit accuracy with a 0.1% mismatch error.

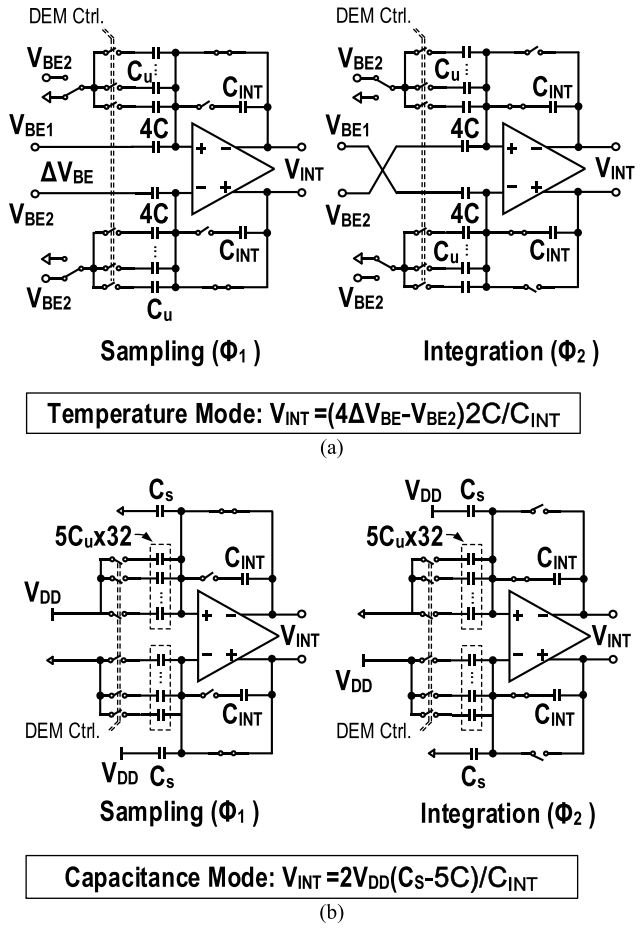


Fig. 6. Operation of sampling and integration in (a) temperature, and (b) capacitance sensing modes.

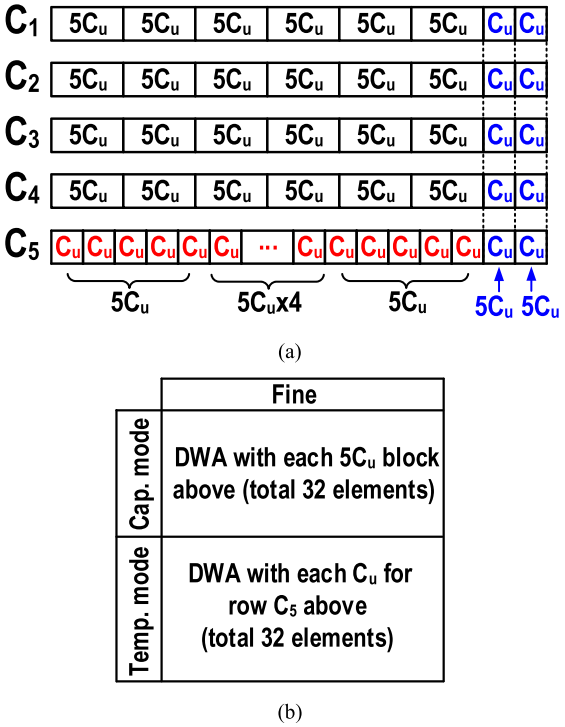


Fig. 7. Block-based DWA Control: (a) capacitor bank segmentation; and (b) DWA control in fine conversions for both modes.

In this work, a coarse resolution of 5-b is optimal to achieve an overall resolution of 15-b based on our study in section II-B. As illustrated in Fig. 7(b), BDWA only operates in fine conversion according to the coarse output for both modes. In capacitance sensing mode, BDWA operates with a total of 32 $5C_u$-blocks. In temperature sensing mode, a total of 32 C_u in C_5 are switched between ground and V_{BE}, while the other four banks C_{1-4} are connected to ΔV_{BE}. Due to the incomplete cycling of all the DEM elements, a residual gain error in K exists between the coarse and fine conversions, degrading the temperature sensing accuracy. Simulation results show that this error leads to a change of $\sim$0.015% in α, which is below the error bound of 0.02% as set by the target accuracy of 0.2 °C.

D. Complete Circuit

Fig. 8 shows the simplified schematic of the proposed capacitive sensor readout with the corresponding timing diagram. The input capacitance (C_s) and temperature ($V_{BE1,2}$) signals are multiplexed by the control signal '*sel*'. The readout can operate either as a fully-differential mode or a single-ended mode (by connecting one of the sensing terminals to the common-mode voltage) to facilitate most sensing applications. A coarse conversion cycle $N_C = 16$ is utilized to obtain the 5-bit coarse code D_C, which will be further employed to adjust the reference for fine conversion. Before each conversion, both integrators are reset. DEM controls the switching of the CDAC in fully differential mode, denoted as $S_{T_p,n}$ and $S_{C_p,n}$. The two-step I-ADC operates at an oversampling frequency of 2 kHz. The $1/f$ noise and offset of the amplifier are mainly suppressed by the correlated double sampling (CDS) technique. It utilized two non-overlapping clocks $\varphi 1$ and $\varphi 2$, as shown in Fig. 8. During $\varphi 1$, the $1/f$ noise and offset of the amplifier are sampled, which are effectively cancelled during the signal integration phase $\varphi 2$. The induced noise-folding in CDS will inevitably increase the near-DC noise floor, which should be carefully considered in the implementation. System level chopping at 250 Hz is also utilized to further suppress the residual offset [34], [35].

For the integrator, the finite DC gain of the amplifier will lead to integrator leakage and introduce dead zone. Simulation results show that the SQNR begins to degrade when the DC gain of the amplifier falls below 62 dB. As a result, the amplifier gain is designed to be $>$68 dB (typically 82.6 dB) to guarantee the SQNR over PVT variations via Monte-Carlo simulations. Unlike the popular inverter-based amplifier [24], [31] which draws large instantaneous current that would overburden wireless/implantable pressure sensing systems with limited power/energy resources, this work employs a subthreshold biased two-stage amplifier drawing constant current at nA level. Indirect compensation approach via split-length devices [23] is adopted by connecting the compensation capacitor C_c to an internal low impedance node in the first stage. Compared with the traditional Miller compensation approach, the non-dominant pole can be boosted

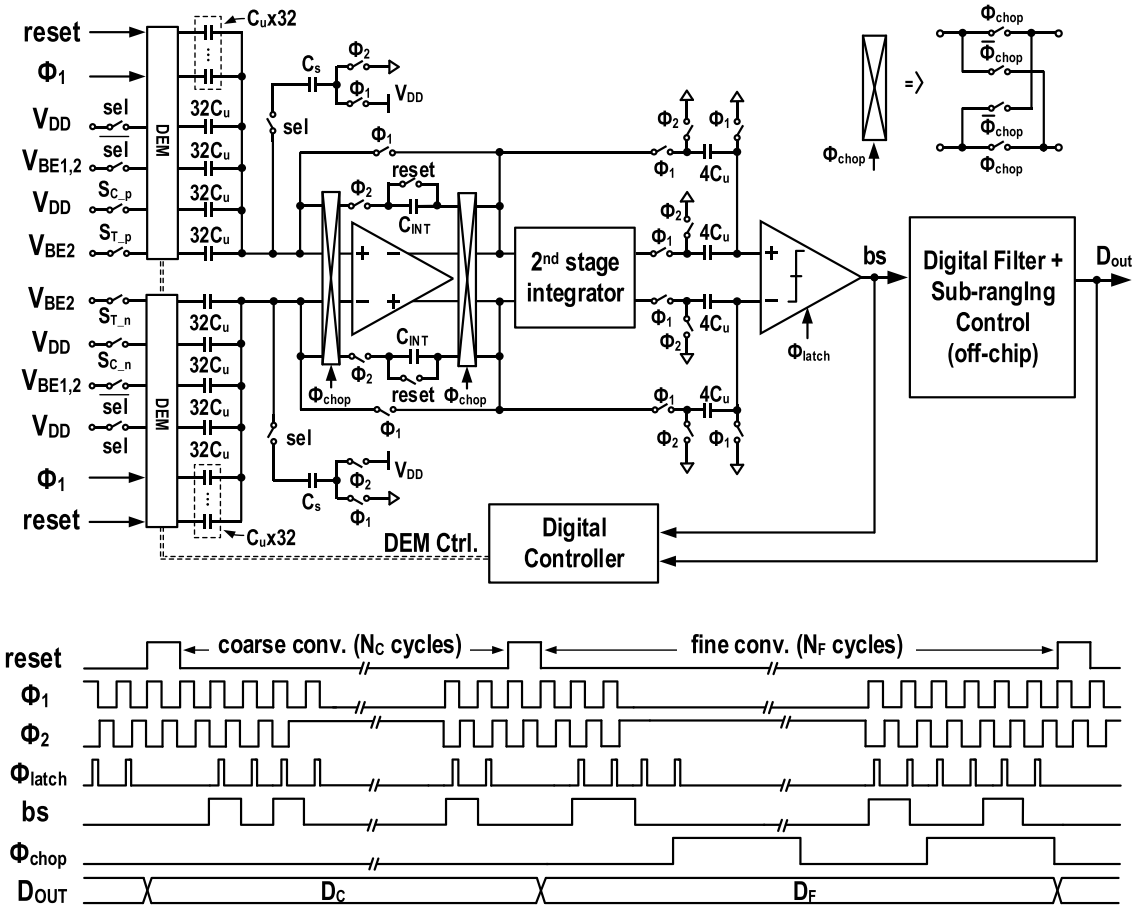


Fig. 8. Detailed schematic of the readout circuit and timing diagram.

by a factor of C_c/C_A, where C_A denotes the capacitance at node A in Fig 9. Essentially, the power consumption can be optimized by increasing C_c while ensuring the close-loop stability. Based on the nW power budget, we reduced the power in the second stage, which draws comparable current with the first stage (∼36 nA) while fulfilling both the settling and stability requirements with C_c equals to 0.9 pF. The achieved DC gain, GBW and phase margin are 82.6 dB, 24 kHz and 61° with an effective loading of 10 pF, respectively. These performances are sufficient for the 15-bit I-ADC to operate at an oversampling frequency of 2 kHz. The amplifier only consumes a total power of 114 nW, including the common-mode feedback (CMFB) circuit.

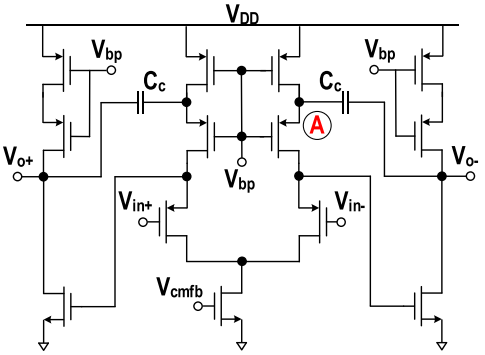


Fig. 9. Schematic of the two-stage amplifier in the integrators.

IV. Measurement Results

An experimental prototype of the proposed capacitive MEMS readout circuit has been fabricated in a standard 0.18-μm 1P6M CMOS technology. It occupies an active area of 0.18 mm^2, with the biasing circuit and BJT-core, two-step I-ADC with clock generation block, and the digital control logic as shown in Fig. 10(a). The digital filter and sub-ranging control is implemented in FPGA for flexibility. The performance of the chip is evaluated experimentally using a discrete trimmable capacitor (MAX1474). Table II gives the measured power breakdown at room temperature. The BJT-core is turned off in capacitance sensing mode. Fig. 11 shows the measured power consumption via 15 chips. The averaged power consumptions for capacitance and temperature sensing modes are 549 nW and 703 nW under 1-V supplies (one for digital and one for analog).

For the capacitance measurement, we calibrated the trimmable capacitor IC (MAX1474, Maxim) down to an accuracy of <0.04 fF using the precision LCR meter (E4980A). The discrete capacitor is connected to the input of the readout in differential mode to minimize the PCB parasitics. The measured capacitance accuracy is ±0.17 fF (1σ) via 15 chips, which corresponds to 14.1 bits from 0 to 10.8 pF as shown

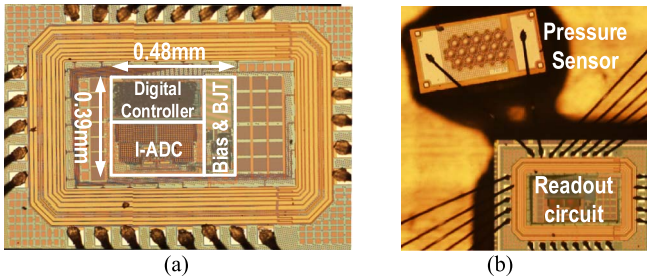


Fig. 10. (a) Die photo of the proposed capacitive sensor readout. (b) Assembly of the MEMS pressure sensor and the readout circuit.

TABLE II
MEASURED POWER BREAKDOWN AT ROOM TEMPERATURE

Building Block	Power Consumption at Room Temperature	
	Cap. Mode	Temp. Mode
Bias & BJT-core	117 nW (BJT core turned off)	252 nW
Ctrl. Logic	143 nW	143 nW
Clock Gen.		
DAC	283 nW	298 nW
1st Integrator		
2nd Integrator		
Comparator		
Total	**543 nW**	**693 nW**

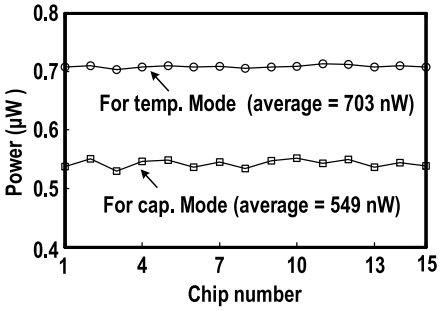


Fig. 11. Measured power consumption of capacitance and temperature sensing modes (15 chips).

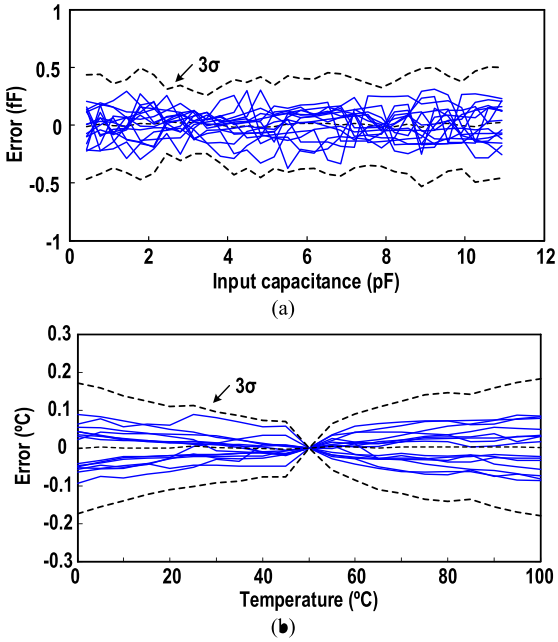


Fig. 12. (a) Measured capacitance error via 15 chips after individual calibration, with bold dashed lines indicating the $\pm 3\sigma$ bounds. (b) Measured temperature error via 15 chips after one-point calibration at 50 °C, with bold dashed lines indicating the $\pm 3\sigma$ bounds.

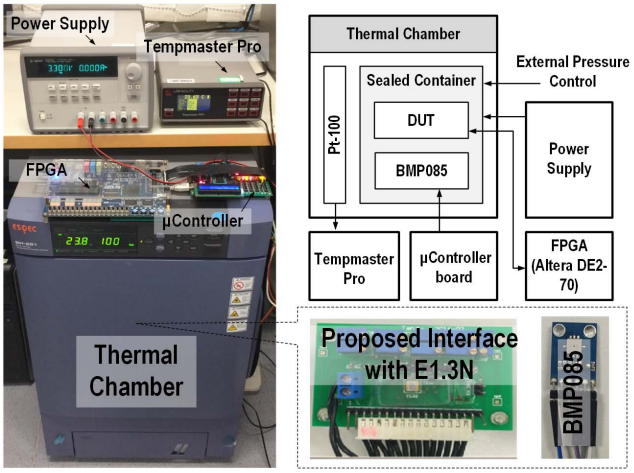


Fig. 13. System measurement setup of the proposed capacitive sensor readout.

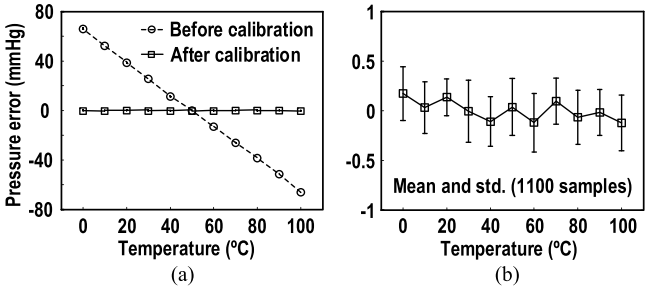
in Fig. 12 (a). We also measured 15 chips over the temperature range from 0 to 100 °C inside a thermal chamber (SU-261). The device under test (DUT) is placed next to a temperature reference (a Pt-100 resistor calibrated with ±0.02 °C accuracy) inside a metal box which severs as a thermal low-pass filter. The reference temperature from Pt-100 is obtained by Tempmaster Pro (by Labfacilicity). As shown in Fig. 12(b), the measure temperature inaccuracy is ±0.18 °C (3σ) after one-point trimming at 50 °C using a linear master curve. The reduced resolution in the temperature mode is mainly due to the nonlinear relationship of $\Delta V_{BE}/V_{BE}$ over the entire temperature range. In addition, the sensing accuracy will be degraded at low temperature due to the insufficient headroom in the biasing circuit [36], which can be resolved by increasing the supply voltage at the cost of increased power dissipation.

For system level characterization, we packaged the proposed system with an off-chip MEMS pressure sensor (E1.3N by MicroFab) as shown in Fig. 10(b). Fig. 13 illustrates the system level measurement setup. BMP085 (by Bosch), which is controlled by the microcontroller, serves as the reference pressure sensor with a resolution of 7.5×10^{-3} mmHg. The decimation filter, sub-ranging control and data logging are implemented using the FPGA board (Altera DE2-70), and the introduced delay of around 2.5 μs is negligible in the feedback loop regarding the clock period of 500 μs. Mixed-signal simulation shows that the sinc^2 digital filter and the sub-ranging controller introduce an area overhead of less than 4.5%, and a power overhead of 3.8% and 3% for the capacitance and temperature modes, respectively. During measurement, both the DUT and BMP085 are placed in a sealed container, which is then put inside the temperature chamber. The pressure in the sealed container is controlled

TABLE III
PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ARTS

Parameters	PCAP02 [37]	AD7747 [22]	JSensor'15 [4]	JSensor'16 [14]	VLSI'17 [11]	This work
Tech. (μm)	N/R	N/R	0.18	0.18	0.16	0.18
Topology	Period Modulation	I-ADC	C-V+SAR ADC	Period Modulation	SAR+I-ADC	Two-step I-ADC
Temperature calibration method	On-chip Temperature Sensor	On-chip Temperature Sensor	On-chip Temperature Sensor	Temperature Compensation	On-chip Temperature Sensor	On-chip Temperature Sensor
Supply voltage (V)	3	3.3	1.8	0.8	1.8	1
Temp. range (°C)	-20 to 60	-40 to 125	N/R	-40 to 125	-55 to 125	0 to 100
Temp. accuracy (°C)	±0.1	±0.2	N/R	N/R	±0.2	±0.18 (3σ)
Temp. resolution (°C)	0.025	0.1	N/R	N/R	0.004	0.04
Input range (pF)	10 to 11	-8 to 8	3.4 to 4.2	6.41 to 9.77	0 to 3.8	0 to 10.8
Cap. resolution (fF)	0.11	0.19#	±2.5(1σ)	2.05	0.0025	±0.17 (1σ)
Meas. time (ms)	400^	22#	0.02	17.5	100	40
P_{temp} (μW)	7.5^	2310	N/R	N/R	8.3§	**0.72&**
P_{cap} (μW)			70	18.4	8.3§	**0.57&**
ENOB (bits)	11.3^	14.3#	7.3*	10.4*	18.7	14.1
Area (mm^2)	N/R	N/R	1.2	0.1	0.33	**0.18**
FoM_{cap} (pJ/conv.-step)	1190^	2519#	9.7	238	0.79	1.3
FoM_{acc} ($nJ\%^2$)	188	2987	N/R	N/R	40	3.7
FoM_{res} ($pJ°C^2$)	1875	254100	N/R	N/R	8	46

* Extracted from the corresponding literature
\# Extracted data for low power consumption mode
§ Power for digital filter not included
^ Extracted data for similar capacitance resolution
& Estimated power for digital controller included



(a) (b)

Fig. 14. System level measurement: (a) pressure accuracy before and after temperature compensation; and (b) close-up after calibration.

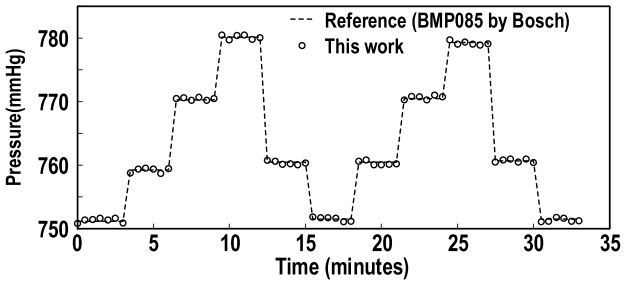


Fig. 15. Dynamic pressure measurement with a reference pressure sensor.

externally. The DUT is calibrated by varying the environment pressure under different temperature settings (10°C steps from 0 to 100°C), and the resultant lookup table is utilized for real time calibration using linear interpolation. Fig. 14 shows that a $>150\times$ improvement in the measured pressure error (reduced from ±67 mmHg to ±0.44 mmHg) is achieved after temperature compensation. The standard deviation is less than 0.5 mmHg with 100 measurements taken at each temperature. The pressure accuracy is 0.34 mmHg (1σ) over the entire temperature range, making it suitable for practical wireless sensing applications. Fig. 15 shows the dynamic performance with respect to a reference pressure sensor, and the measured standard deviation is 0.29 mmHg.

We benchmark our work with similar sensor interfaces with built-in temperature compensation as in Table III, in which the FoM_{cap} is calculated as [9]

$$FoM_{cap} = \frac{P \times T_{meas.}}{2^{ENOB}}, \tag{9}$$

where P is the power consumption, $T_{meas.}$ denotes the conversion time in one measurement, and *ENOB* is the effective number of bits given as in (10)

$$ENOB = \frac{20\log\left(\frac{Input\ range}{2\sqrt{2}\times Cap.res.}\right) - 1.76}{6.02}. \tag{10}$$

The resolution FoM (FoM_{res}) and accuracy FoM (FoM_{acc}) are defined as [31]

$$FoM_{res} = P \times T_{meas.} \times Resolution^2, \tag{11}$$

$$FoM_{acc} = P \times T_{meas.} \times \left(100 \times \frac{Max.Error}{Temp.\ range}\right)^2. \tag{12}$$

When compared with capacitive sensing systems with temperature calibration in both commercial products [22], [37] and literatures [4], [14], this work achieves nW power consumption with similar capacitance and temperature accuracies, which is benefited from the improved linearity and intrinsic property of the two-step I-ADC with optimal coarse/fine bit allocations. Although [11] achieves >60% better energy efficiency, it essentially burns $>10\times$ higher power while occupying >80% larger area using similar technology nodes. Finally, the proposed sensor interface with built-in temperature sensor achieves the highest power efficiency, competitive FoM_{cap},

FoM_{res} and FoM_{acc}, and compact area, making it suitable for those energy- and area-constrained systems.

V. Conclusion

This work demonstrates a nano-watt class high accuracy capacitive sensor readout with on-chip temperature drift compensation by reusing an energy-efficient incremental ADC, achieving the state-of-the-art performance. More importantly, we introduce a systematic investigation on the optimal coarse/fine bit allocations for two-step I-ADCs in the presence of mismatch errors, and reveal that they even result in inferior performance when compared with the conventional I-ADC. The fabricated prototype was individually characterized for capacitance and temperature sensing modes, and also packaged with a commercial MEMS pressure sensor for system level validation. The competitive performance makes it a promising candidate for energy-efficient high accuracy capacitance sensing applications.

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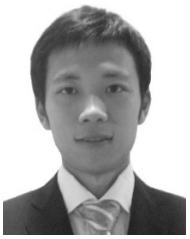

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