Algorithmic Voltage-Feed-In Topology for Fully Integrated Fine-Grained Rational Buck–Boost Switched-Capacitor DC–DC Converters

Yang Jiang, *Student Member, IEEE*, Man-Kay Law, *Senior Member, IEEE*, Pui-In Mak, *Senior Member, IEEE*, and Rui P. Martins, *Fellow, IEEE*

***Abstract*— We propose an algorithmic voltage-feed-in (AVFI) topology capable of systematic generation of any arbitrary buck–boost rational ratio with optimal conduction loss while achieving reduced topology-level parasitic loss among the state-of-the-art works. By disengaging the existing topology-level restrictions, we develop a cell-level implementation using the extracted Dickson cell (DSC) and charge-path-folding cell (QFC) to minimize the power-stage parasitic loss, exhibiting a Dickson-like switching pattern. The proposed partitionable main cell (MC) and auxiliary cell (AC) architecture achieves fined-grained voltage conversion ratio (FVCR) reconfiguration with optimal power cell utilization and reduced control complexity. Implemented in 65-nm bulk CMOS, the fully integrated switched-capacitor power converter (SCPC) using 10 MCs and 10 ACs executes a total of 24 VCRs (11 buck and 13 boost) with wide-range efficient buck–boost operations through the proposed reference-selective bootstrapping driver (RSBD). Based on the AVFI topology, the chip prototype reaches a measured peak efficiency of 84.1% at a power density of 13.4 mW/mm^2 over a wide range of input (0.22–2.4 V) and output (0.85–1.2 V).**

***Index Terms*— Algorithmic voltage-feed-in (AVFI) topology, buck–boost, dc–dc, linear topology, parasitic loss, power density, rational voltage conversion ratio, reconfigurable, reference-selective bootstrapping, switched capacitor.**

I. Introduction

EFFICIENT wireless energy harvesting solutions are highly demanded in many portable dynamically powered internet of everything (IoE) systems. Switched-capacitor power converters (SCPC) are desirable for on-chip dc–dc conversion due to its full integration capability with high energy efficiency and power density [1]–[18]. Due to the wide input–output dynamics as a result of the changing ambient environment, SCPC with multiple voltage conversion ratios (VCR) is necessary to alleviate the VCR-induced efficiency penalty while achieving a small form factor [19]–[30]. Yet, many existing works offer only a few VCRs, leading to significant efficiency fluctuations over wide input–output dynamics (e.g., up to 30% in [28]). Hence, on-chip SCPCs with systematic fine-grained VCRs (FVCRs) become attractive to achieve consistent high efficiency across an extended operating range [7], [31]–[34]. Even though glitches and hard-charging losses can result during VCR reconfiguration, such issues should be much relaxed for the target application scenario.

Conventionally, the Dickson topology has been widely employed in many fully integrated step-up/-down solutions with high efficiency due to its optimal bottom-plate (C_{bot}) parasitic loss [35], [36]. However, it can only achieve 1-to-n (1:n) boost VCRs and n-to-1 (n:1) buck VCRs due to its topology inflexibility, rendering FVCR implementations impossible. As an alternative, the series–parallel (SP) topology is well known for its VCR flexibility [37] but is not preferred for on-chip implementations due to the suboptimal slow-switching loss [38] (i.e., R_{SSL}) and C_{bot} parasitic loss.

To overcome the limitations as demonstrated in the Dickson and SP topologies, various systematic rational VCR generation techniques based on binary converters have recently been proposed to achieve fined-grained resolution including the successive approximation register (SAR) SCPC [31], recursive SCPC (RSC) [32] [33], and negator-feedback SCPC (NSC) [34]. Due to their intrinsic binary switching property, each flying capacitor carries binary-weighted charge flow, with each stage performing either voltage doubling or halving steps. Even though they can achieve less number of power cell stages for generating high conversion ratios, its binary stepping characteristics can increase the C_{bot} switching voltage (ΔV_{CB}), raising the on-chip flying capacitor (C_{fly}) parasitic loss which can significantly degrade the power conversion efficiency. As a performance tradeoff, existing works mostly employ metal–insulator–metal (MIM) capacitors with low C_{bot} as the energy storage elements but at the expense of limited power density in the order of sub-mW/mm^2 [7], [25]–[26], [31]–[34].

This paper (expanded from [39]) revisits the fundamental properties of the traditional Dickson and SP topologies and proposes a systematic SCPC topology design methodology to achieve optimal power stage losses. The proposed method includes a core framework featuring the algorithmic voltage-feed-in (AVFI) function to achieve linear topologies

Manuscript received May 3, 2018; revised July 12, 2018 and August 9, 2018; accepted August 20, 2018. Date of publication September 27, 2018; date of current version December 21, 2018. This paper was approved by Guest Editor Tai-Haur Kuo. This work was supported in part by the Macao Science and Technology Development Fund under Grant FDCT069/2016/A2 and in part by the Research Committee of the University of Macau under Grant MYRG2018-00196-AMSV. *(Corresponding author: Man-Kay Law.)*

Y. Jiang and P.-I. Mak are with the State Key Laboratory of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau, Macau 999078, China (e-mail: yang.jiang@connect.umac.mo; pimak@umac.mo).

M.-K. Law is with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau 999078, China (e-mail: mklaw@umac.mo).

R. P. Martins is with the State Key Laboratory of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau, Macau 999078, China, on leave from the Instituto Superior Técnico, Universidade de Lisboa, 1049-001 Lisbon, Portugal (e-mail: rmartins@umac.mo).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2018.2866929

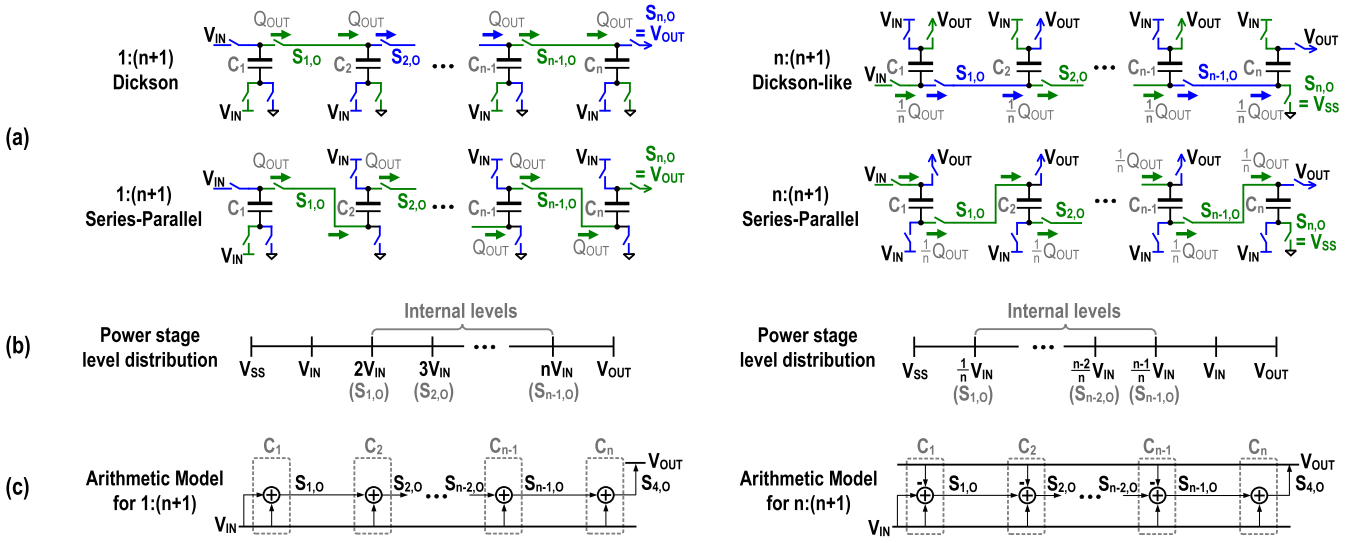


Fig. 1. (a) Demonstration of 1:$(n+1)$ and n:$(n+1)$ conversions by conventional Dickson and SP topologies, (b) their corresponding power stage internal generated levels, and (c) their respective arithmetic model representations.

for flexible rational VCR generations with optimal R_{SSL}. The proposed AVFI framework, together with the Dickson cell (DSC) and the charge-folding cell (QFC) which are extracted from the existing Dickson and SP topologies, can algorithmically attain improved parasitic loss for any arbitrary rational VCR among the state of the art. While a charge recycling technique is presented in [10], the proposed AVFI topology achieves parasitic loss reduction at the topology level. Both techniques should theoretically be compatible with each other but at the expense of increased circuit and control complexity. Using the proposed methodology, a fully integrated buck–boost SCPC with 24 VCRs was implemented in 65-nm bulk CMOS. Due to the intrinsic unit charge flow property, modular power cells can be adopted to relax the implementation/control complexity. A partitionable power stage containing 10 main cells (MCs) and 10 auxiliary cells (ACs) with a scaled size ratio of 5 is employed to guarantee full capacitor utilization, with the seven partitioning modes supporting 24 VCRs. To support reliable power switch on/off operations under wide voltage dynamics in FVCR implementations, we also propose a reference-selective bootstrapping driver (RSBD) technique featuring an adaptive selection of the proper gate driving reference node across the power switch for accurate switch-on/-off control while ensuring robust operation using low-voltage power switches to reduce the switching loss.

The organization of this paper is as follows. Section II details the proposed AVFI topology design methodology. Section III presents the corresponding topology analyses. Section IV provides application examples to demonstrate the utilization and characteristics of the proposed topology design technique. Section V outlines the converter design and implementation. Section VI shows the experimental results. Finally, Section VII draws the conclusion.

II. Algorithmic Voltage-Feed-In Topology

A. Conventional Linear Topologies

Dickson-type converters are often referred to as linear with: 1) each power cell carrying uniform charge flow (Q_C) through the flying capacitor (C_{fly}); and 2) the generated internal voltage levels equally distributed within the voltage conversion domain, which is [V_{SS}, V_{IN}] for buck mode and [V_{SS}, V_{OUT}] for boost mode. Fig. 1(a) and (b) illustrates the above-mentioned observations for an n-stage Dickson topology in boost conversion for 1:$(n+1)$ and n:$(n+1)$. For comparison, they also show the SP implementations for the same VCRs. By inspection, the corresponding SP also satisfies the above-mentioned linear topology characteristics. As a result, we can essentially consider SP as an alternative to Dickson in such a scenario. With reference to the existing analysis for Dickson converters [35], [40], we can express the ith stage output level ($S_{i,O}$) in terms of the capacitor voltage $V_{C,i}$ and the bottom-plate switching voltage $\Delta V_{\mathrm{CB},i}$, as

$$S_{i,O,1:(n+1)} = V_{C,i} + |\Delta V_{\mathrm{CB},i}| \tag{1}$$

$$S_{i,O,n:(n+1)} = V_{\mathrm{OUT}} - (V_{C,i} + |\Delta V_{\mathrm{CB},i}|). \tag{2}$$

From Fig. 1(a), the first-stage operation for both topologies and their corresponding output $S_{1,O}$ are the same, with the later stage results depending on the previous stages. Even though they can both generate the same set of voltage levels using the same number of capacitors, their unique charge pumping characteristics can lead to distinct performance advantages/disadvantages. Considering the boost conversion of 1:$(n+1)$ and n:$(n+1)$, the Dickson and SP voltage stepping characteristics are, respectively, given as

$$1:(n+1)\begin{cases}\text{Dickson}: & V_{C,i} = S_{i-1,O},\ |\Delta V_{\mathrm{CB},i}| = V_{\mathrm{IN}} \\ \text{SP}: & V_{C,i} = V_{\mathrm{IN}},\ |\Delta V_{\mathrm{CB},i}| = S_{i-1,O}\end{cases} \tag{3}$$

$$n:(n+1)\begin{cases}\text{Dickson}: & V_{C,i} = V_{\mathrm{OUT}} - S_{i-1,O} \\ & |\Delta V_{\mathrm{CB},i}| = V_{\mathrm{OUT}} - V_{\mathrm{IN}} \\ \text{SP}: & V_{C,i} = V_{\mathrm{OUT}} - V_{\mathrm{IN}} \\ & |\Delta V_{\mathrm{CB},i}| = V_{\mathrm{OUT}} - S_{i-1,O}\end{cases} \tag{4}$$

From (3) and (4), the Dickson topology features fixed $\Delta V_{\mathrm{CB},i} = V_{\mathrm{IN}}$ or V_{OUT}–V_{IN}. Intuitively, this operation leads to its stage by stage increase in capacitor voltage. In contrast, each C_{fly} in the SP topology has fixed voltage $V_{C,i} = V_{\mathrm{IN}}$ or

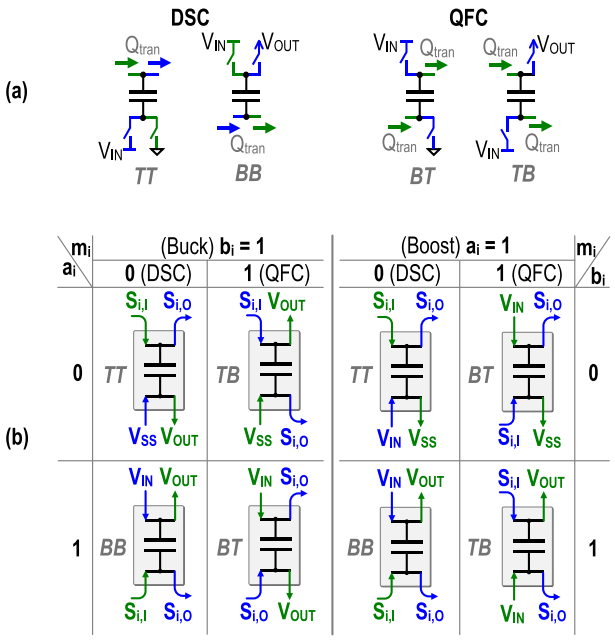


Fig. 2. (a) Extracted power cells from Dickson and SP boost topologies. (b) Summary of basic power cells used in the proposed topology design method.

V_{OUT}–V_{IN} but with gradually increased $\Delta V_{\mathrm{CB},i}$. As demonstrated in [35] and [36], the Dickson topology can theoretically achieve the minimum parasitic loss for a particular VCR, and is therefore a preferred solution when compared with SP. However, as $V_{C,i}$ solely relies on the previous stage outputs which can only be multiples of V_{IN} or V_{OUT}–V_{IN}, conventional Dickson converter only generates limited VCRs of 1:$(n+1)$ and n:$(n+1)$ in boost conversion, equivalent to $(n+1)$:1 and $(n+1)$:n in buck mode. Furthermore, for the special case SP which realizes VCRs of 1:$(n+1)$ and n:$(n+1)$ in Fig. 1(a), the voltage-stepping amplitude $\Delta V_{\mathrm{CB},i}$ also limits the realizable VCRs as in the Dickson case.

The aforementioned power stage-level generation can be represented by the arithmetic model of Fig. 1(c). By inspection, except for the last stage, there is no V_{OUT} involvement in the operations of all the other stages for 1:$(n+1)$ generation. In contrast, all the power cells rely on V_{OUT} for n:$(n+1)$ conversion. We can observe that the performance limitations in existing Dickson and SP topologies are mainly due to their inherent converter operations, which are ultimately defined by the voltage stepping characteristics of the corresponding power cells. Based on the above-mentioned observation, we propose the AVFI topology that exploits the basic cell characteristics of both the Dickson and SP topologies. This essentially disengages their respective topology-level restrictions, resulting in flexible rational VCR generations with optimal R_{SSL} and parasitic loss performances.

B. Basic Power Cells

Referring to the Dickson and SP boost topologies of Fig. 1(a), we extract the basic power cells to construct the proposed topology in this paper, including two DSCs and two QFCs from the Dickson and SP topologies, respectively, as shown in Fig. 2(a). As summarized in Section II-A, the DSC achieves predictable $\Delta V_{\mathrm{CB}} = V_{\mathrm{IN}}$ or $|V_{\mathrm{OUT}}–V_{\mathrm{IN}}|$.

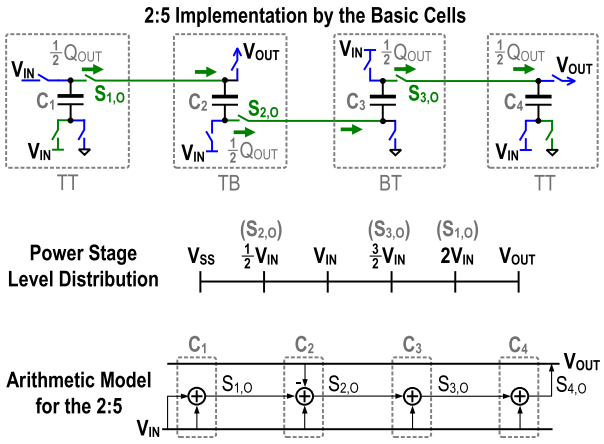


Fig. 3. Topology exploration for rational VCR of 2:5.

Fig. 2(a) also presents the charge transfer (Q_{tran}) pattern of C_{top}-in-C_{top}-out (TT) or C_{bot}-in-C_{bot}-out (BB). In contrast, the ΔV_{CB} for the QFC depends on internal node conditions of adjacent power cells, with Q_{tran} "folding" to the opposite plate, showing C_{top}-in-C_{bot}-out (TB) or C_{bot}-in-C_{top}-out (BT). The above-mentioned patterns distinguish the four basic power cells for boost conversion. Similarly, basic cells can also be extracted from the buck conversion cases. Fig. 2(b) summarizes the total of eight basic power cells for buck–boost conversion, with cell parameter m_i introduced to differentiate between DSC ($m_i = 0$) and QFC ($m_i = 1$). Furthermore, the basic power cells can also be characterized by the employment of output/input voltage-feed-in (VFI), i.e., the involvement of charges transferred to V_{OUT} in boost mode and injected from V_{IN} in buck mode. For instance, the arithmetic model for 1:$(n+1)$ in Fig. 1(c) exhibits no V_{OUT}-feed-in for all power cells. In contrast, all the power cells for n:$(n+1)$ require V_{OUT}-feed-in operation. Consequently, to further classify the basic power cells, we defined a_i and b_i as the V_{IN}-feed-in and V_{OUT}-feed-in parameters, respectively. Hence, $V_{\mathrm{IN}}(V_{\mathrm{OUT}})$-feed-in is involved when a_i $(b_i) = 1$ and vice versa. With the above-mentioned topology parameters (i.e., VFI parameters a_i and b_i and cell selection parameter m_i), every power cell among the total of eight shown in Fig. 2(b) can be uniquely addressed.

Fig. 3 exhibits, for a better understanding, how the basic cells can be applied for rational VCR generation. It illustrates a 2:5 boost conversion example whose implementation is based on the selected cells from the boost mode basic cell set. For a given $V_{\mathrm{IN}} = 2$, the corresponding $V_{\mathrm{OUT}} = 5$ can be generated using a TT cell as C_4 if $S_{3,O} = 3$. A possible solution is to set the previous stages C_{1-3} using TT/BT, TB, and BT cells, resulting in $S_{1-3,O} = 4$, 1, and 3, respectively. Fig. 3 also displays the power stage voltage-level distribution for the derived 2:5 topology which is able to achieve optimum R_{SSL} as well as C_{bot} parasitic loss.

Notice that the VFI parameters a_i and b_i essentially determine the generated VCR, which will be discussed in the AVFI framework in Section II-C. However, as either the DSC ($m_i = 0$) or QFC ($m_i = 1$) can theoretically support the specific implementation for the power cells in the framework (but can affect the value of ΔV_{CB} of each power cell

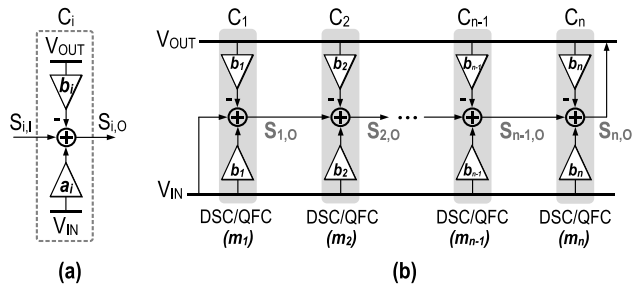


Fig. 4. Algorithmic models for (a) power cell and (b) topology framework.

and hence the parasitic loss), the complete AVFI topology implementation requires the complete topology parameter selection (i.e., a_i, b_i, and m_i), outlined in Section II-D.

C. Proposed AVFI Framework

Compared with the case of 1:5, the arithmetic model of 2:5 introduces an additional VFI path at C_2, resulting in VCR modification. In principle, flexible rational VCR generation can be accomplished by controlling the VFI operation in a topology framework with a given number of cascaded power cells. Essentially, the construction of the arithmetic model is dependent on the $V_{\rm IN}$- and $V_{\rm OUT}$-feed-in operations in each power stage, meaning that both a_i and b_i are necessary for the general model representation. Moreover, for a particular VCR, the value of a_i and b_i is not unique, with each solution achieving different sets of $\Delta V_{{\rm CB},i}$. The proposed algorithmic AVFI topology aims to determine the VFI parameters a_i and b_i as well as the cell parameter m_i systematically through an algorithmic framework to obtain VCR flexibility and optimal losses.

As discussed, flexible rational VCR generation can be achieved through programming the VFI paths from the converter input ($V_{\rm IN}$) and output ($V_{\rm OUT}$) to each power cell stage. Consequently, the topology implementation is VCR specific, which is dependent on the particular set of VFI enforced. As the AVFI framework with a_i and b_i inherently maintains the characteristics of linear topologies, it leads to an intrinsic optimal $R_{\rm SSL}$ for any arbitrary VCR generation. Notice that this step does not require the selection between the DSC/QFC cells (i.e., the choice of m_i).

Fig. 4(a) shows the general model of a power cell for VFI parameter determination (i.e., a_i and b_i), describing the functional voltage conversion within a power cell. The ith stage cell output can be expressed as

$$S_{i,O} = S_{i,\rm I} + a_i V_{\rm IN} - b_i V_{\rm OUT}, \begin{cases} b_i = 1 (\text{buck}) \\ a_i = 1 (\text{boost}). \end{cases} \tag{5}$$

Since all DSCs and QFCs process arbitrary cell input voltage $S_{i,I}$ by either acquiring charge from $V_{\rm IN}$ or delivering charge to $V_{\rm OUT}$, the cell model can algorithmically express the cell function by a_i and b_i in (5). Fig. 4(b) reveals the generalized algorithmic topology framework through cascading the cell models in Fig. 4(a). From Fig. 4(b), $S_{i,O}$ is an accumulative result of previous stages, with the general expression

$$S_{i,O} = \left(1 + \sum\nolimits_{j=1}^{i} a_j\right) V_{\rm IN} - \left(\sum\nolimits_{j=1}^{i} b_j\right) V_{\rm OUT}. \tag{6}$$

By assuming $S_{n,O} = V_{\rm OUT}$, the proposed framework can realize any arbitrary buck–boost VCRs, given by

$$\text{VCR} = \frac{V_{\rm OUT}}{V_{\rm IN}} = \frac{1 + \sum a_{1\sim n}}{1 + \sum b_{1\sim n}}, \begin{cases} a_1 = 0, b_{1\sim n} = 1 \text{ (buck)} \\ a_{1\sim n} = 1, b_n = 0 \text{ (boost)} \end{cases} \tag{7}$$

For an n-stage converter, setting all $a_i = 1$ in boost mode can set the numerator to be $n + 1$, ensuring proper VCR generation from n:$(n+1)$ to 1:$(n+1)$ through different values of b_i. This is analogous for setting all $b_i = 1$ in buck mode. Consequently, we can ensure proper VCR generation between $(n + 1)$:x and x:$(n + 1)$, where x is any positive integer with $1 \le x \le n$. We assume non-unity VCR generation by setting a_1 in buck and b_n in boost to be 0. The resultant converter can also achieve optimal $R_{\rm SSL}$, which is analogous to the conventional Dickson and SP converters and will be detailed in Section III-A. In fact, the 1:$(n + 1)$ and n:$(n + 1)$ Dickson topologies can also be considered as special cases of the proposed AVFI topology framework. In summary, any particular VCR can be theoretically generated by properly defining a_i and b_i.

D. Proposed AVFI Topology With Parameter Selection

Even though the model in Fig. 4(b) can theoretically generate all realizable VCRs by determining the summation terms in (7), the real implementation also relies on specifying individual values of each parameter a_i, b_i, and m_i for optimal $C_{\rm bot}$ parasitic loss. Here, we present a systematic parameter determination methodology to algorithmically determine a set of unique a_i, b_i, and m_i for concrete power cell implementation in the proposed AVFI topology with optimal $C_{\rm bot}$ parasitic loss.

Referring to the power stage voltage-level distribution for the Dickson/SP topology of Fig. 1, we first enforce the level bounded rule (LBR) for determining a_i and b_i in buck and boost modes, respectively. Consequently, all the internal levels are linearly distributed and well bounded within the corresponding conversion domain, i.e., [$V_{\rm SS}$, $V_{\rm IN}$] for buck mode and [$V_{\rm SS}$, $V_{\rm OUT}$] for boost mode, defined as

$$\begin{cases} \text{buck:} S_{i,O}|_{i\in[1,n)} \in (V_{\rm SS}, V_{\rm IN}) \\ \text{boost:} S_{i,O}|_{i\in[1,n)} \in (V_{\rm SS}, V_{\rm OUT}) \end{cases} \tag{8}$$

Based on the LBR and the $S_{i,O}$ expressions in (5) and (6), we can derive the algorithms for a_i and b_i for the buck and boost conversion as

$$\text{buck}: a_i|_{i\epsilon[2,n]} = \begin{cases} 1, & i \cdot \text{VCR} > 1 + \sum\limits_{j=1}^{i-1} a_j \\ 0, & \text{otherwise} \end{cases} \tag{9}$$

$$\text{boost}: b_i|_{i\epsilon[1,n-1]} = \begin{cases} 1, & \left(1 + \sum\limits_{j=1}^{i-1} b_j\right) \text{VCR} < i + 1 \\ 0, & \text{otherwise} \end{cases} \tag{10}$$

Referring to (7), a_0 and b_n are equal to 0 in buck and boost modes, respectively. Fig. 5 presents the corresponding flow charts for systematic a_i/b_i determination in each cell with

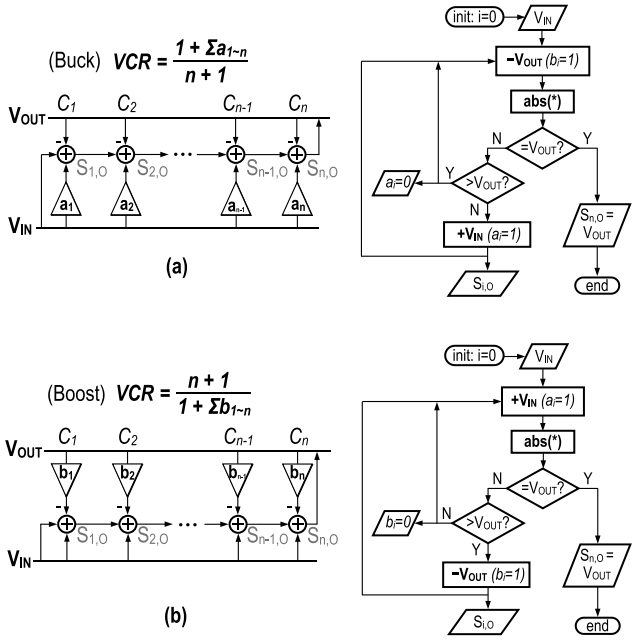


Fig. 5. Algorithm logic flowchart for determining (a) a_i for buck conversion and (b) b_i for boost conversion.

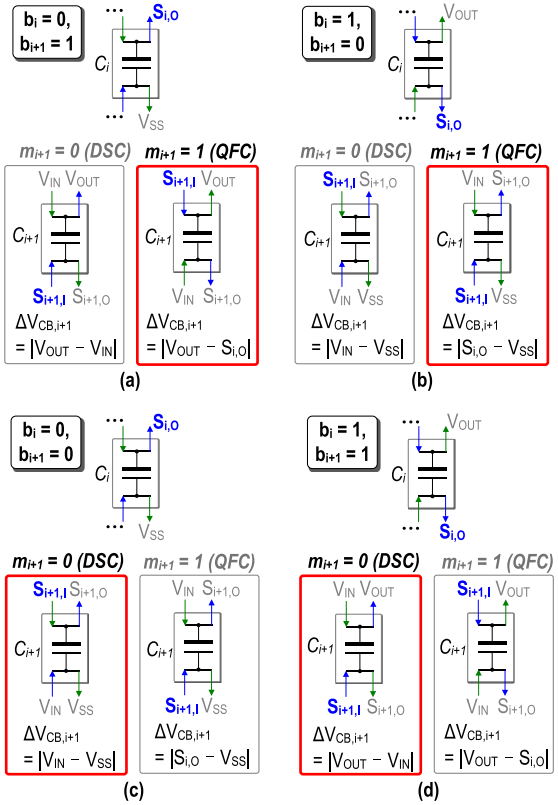


Fig. 6. Power cell selection between DSC and QFC for reduced ΔVCB.

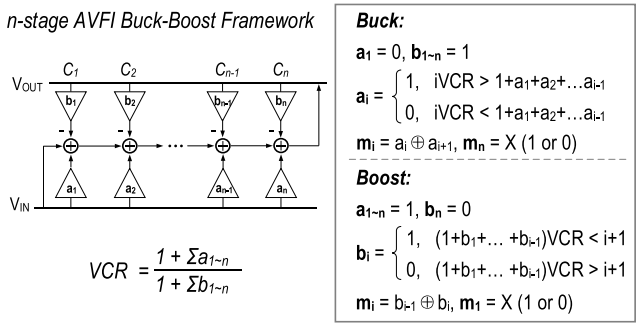


Fig. 7. Complete AVFI topology theory for the rational buck–boost conversion. The cell configuration summary is illustrated in Fig. 2(b).

internal voltages defined. As observed, the parameter determination of the current stage relies on the internal voltage from prior stages only. In other words, the input of any intermediate stages is an accumulating result from earlier stages due to the cell cascading nature, resulting in the accumulative terms of the inequalities in (9) and (10). With the obtained a_i and b_i, it can be observed that the resultant AVFI framework fulfills the linear topology characteristics defined in Section II-A.

Here, we describe the selection algorithm for m_i. As discussed in Section II-A, the unchangeable power cell configurations in conventional topologies are the fundamental reason for either inflexible VCR generation or increased R_{SSL}/parasitic loss. Our proposed framework resolves this problem by enabling identical voltage conversion using different types of power cells. Fig. 6 illustrates the cell selection methodology based on the LBR to optimize the ΔV_{CB} in a particular power cell. Without the loss of generality, we focus our discussion mainly on the boost conversion. Since the input of each intermediate power cell is solely dependent on prior stages, we only need to consider the interfacing of two adjacent intermediate cells, i.e., the four cases for b_i and b_{i+1} as shown in Fig. 6. Referring to Fig. 6(a), $\Delta V_{CB,i+1} = |V_{OUT} - S_{i,O}|$ in steady-state operation for $m_{i+1} = 1$ (QFC). The defined LBR ensures $S_{i,I} > V_{SS} = 0$. In boost mode, $S_{i,O} = S_{i,I} + V_{IN}$ (as $a_i = 1$ and $b_i = 0$), we can have $S_{i,O} > V_{IN}$. Meanwhile, $S_{i,O} < V_{OUT}$ must hold due to LBR. Consequently, we can have $|V_{OUT} - V_{IN}| > |V_{OUT} - S_{i+1,O}|$, and using QFC rather than DSC in the case of Fig. 6(a) always gives lower $\Delta V_{CB,i+1}$. A similar analysis can also be used to deduce the $\Delta V_{CB,i+1}$ for all the possible situations in Fig. 6(b)–(d), as well as for buck mode operations. Then, it can be concluded that by enforcing LBR for the $(i + 1)$th stage, the minimum ΔV_{CB} for cell C_{i+1} can always be achieved with $m_{i+1} = 1$ whenever $b_{i+1} \neq b_i$, and m_{i+1} should be 0 otherwise. The m_i determination algorithm can be expressed as

$$\text{boost}: m_i = b_{i-1} \oplus b_i, \quad m_1 = 0 \text{ or } 1. \tag{11}$$

Since $S_{1,I} = V_{IN}$ for the first stage, the case for $m_1 = 0$ or 1 will result in the same power cell implementation. Similarly, by applying the same selection method in buck mode, the corresponding m_i can be derived as

$$\text{buck}: m_i = a_i \oplus a_{i+1}, \quad m_n = 0 \text{ or } 1. \tag{12}$$

For the last stage C_n, $m_n = 0$ or 1 also gives identical structures as $S_{n,O} = V_{OUT}$ in both cases. The above-mentioned algorithm can be propagated stage by stage to guarantee an optimal parasitic loss at the system level. Fig. 7 summarizes the complete AVFI topology design methodology for the rational buck–boost conversion, including the proposed algorithmic linear topology framework, the generalized VCR expression,

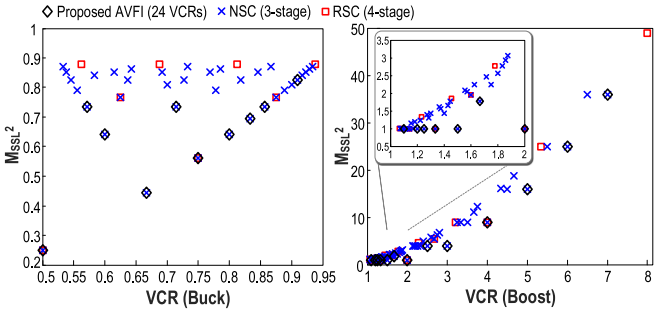


Fig. 8. R_{SSL} comparison between existing topologies and the proposed AVFI framework.

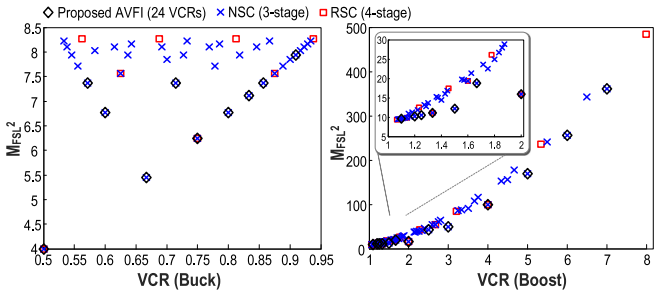


Fig. 9. R_{FSL} comparison between existing topologies and the proposed AVFI framework.

the algorithms for buck–boost VFI parameters a_i/b_i, and cell parameter m_i.

III. Topology Loss Analysis

A. Slow Switching Loss (R_{SSL})

By employing capacitance area-based optimization for C_{fly} assignment [38], the R_{SSL} expression for a generic SC converter topology is given as

$$R_{\text{SSL}} = \frac{1}{C_{\text{TOT}} f_S} M_{\text{SSL}}^2 \tag{13a}$$

$$M_{\text{SSL}} \triangleq \sum_{i \epsilon C_{\text{fly}}} m_{\text{qc},i}. \tag{13b}$$

Here, C_{TOT} is the total C_{fly} and f_S are the operating frequency. In the proposed AVFI framework with n power cells, the normalized capacitor charge multiplier in each cell (also for the existing linear topologies) will become

$$m_{\text{qc},i} \triangleq \left.\frac{Q_{C,i}}{Q_{\text{OUT}}}\right|_{\text{linear}} = \begin{cases} \dfrac{1}{n+1}, & \text{buck VCR} = (n+1):x \\ \dfrac{1}{x}, & \text{boost VCR} = x:(n+1). \end{cases} \tag{14}$$

With a pre-defined area and frequency, R_{SSL} depends solely on the factor M_{SSL}. From the existing SC converter topologies, a VCR-dependent expression for M_{SSL} under minimum R_{SSL} in both buck and boost modes can be summarized as

$$M_{\text{SSL,min}} = \begin{cases} \dfrac{n}{n+1}, & \text{buck VCR} = (n+1):x \\ \dfrac{n}{x}, & \text{boost VCR} = x:(n+1). \end{cases} \tag{15}$$

Based on (14), a linear topology with n power cells theoretically exhibits an M_{SSL} that fulfills the condition in (15). Consequently, the proposed AVFI framework with parameter assignment as defined in (7) can intrinsically achieve an optimal R_{SSL} due to its linear property. By using M_{SSL}^2 as the performance metric, Fig. 8 shows a comparison among the existing binary RSC/NSC topologies and the proposed AVFI topology framework. It can be observed that the proposed technique achieves optimal R_{SSL} similar to the existing state-of-the-art methods.

B. Fast Switching Loss (R_{FSL})

Apart from R_{SSL}, practical power switches also introduce fast switching loss (i.e., R_{FSL} in [38]). By applying the switch area-based optimization [38] for two-phase converters using power switches with one single voltage rating, the corresponding generic R_{FSL} expression will be

$$R_{\text{FSL}} = \frac{2}{G_{\text{TOT}}} M_{\text{FSL}}^2 \tag{16a}$$

$$M_{\text{FSL}} \triangleq \sum_{i \epsilon \text{SW}} m_{\text{qr},i} \tag{16b}$$

$$m_{\text{qr},i} \triangleq \frac{Q_{R,i}}{Q_{\text{OUT}}} \tag{16c}$$

where G_{TOT} is the die-area constrained total switch conductance, $Q_{R,i}$ is the charge passing through the ith switch, and M_{FSL} is a defined factor to evaluate the topology-correlated fast switching loss performance. As discussed, the proposed AVFI topology contains n cells for VCR $= (n+1):x$ or $x:(n+1)$. From Figs. 1 and 3, we can observe that except from the first stage which requires a total of four switches (three connected to known potentials and one connected to next stage), all the other intermediate power stages only require three switches per stage (two connected to known potentials and one to the next stage). For the last stage, it requires three switches all connected to known voltages. In summary, the total number of required switches for an n-stage AVFI converter is

$$N_{\text{SW}} = 4 + 3 \times (n-1) = 3n + 1. \tag{17}$$

Due to the uniform charge flow feature, $Q_{R,i} = Q_{C,i}$ in each cell. By substituting (17) and (16c) into (16b), the M_{FSL} expression for the proposed converter is

$$M_{\text{FSL,AVFI}} = N_{\text{SW}} m_{\text{qr},i} = \begin{cases} \dfrac{3n+1}{n+1}, & \text{buck VCR} = (n+1):x \\ \dfrac{3n+1}{x}, & \text{boost VCR} = x:(n+1). \end{cases} \tag{18}$$

Fig. 9 presents the comparison result for the RSC/NSC and the proposed AVFI topologies, showing that the proposed AVFI topology also reaches equal M_{FSL} under identical VCRs.

C. C_{bot} Parasitic Loss

Apart from the conversion losses induced by R_{SSL} and R_{FSL}, we also need to consider the C_{bot} parasitic loss for fully integrated SCPCs. The corresponding power loss comes

$$P_{\text{ls,par}} = \sum_{i=1}^{n} \beta C_i \Delta V_{\text{CB},i}{}^2 f_S = \beta C_{\text{TOT}} f_S V_{\text{IN}}^2 M_{\text{par}} \tag{19a}$$

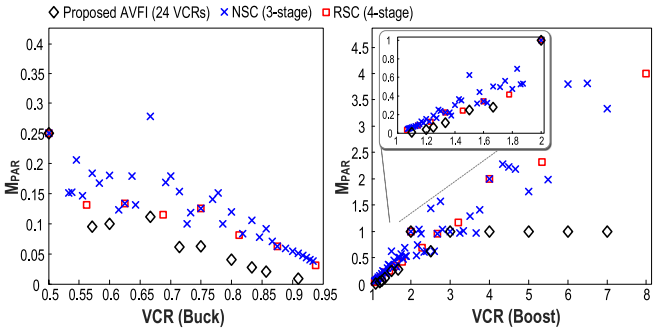


Fig. 10. Comparison of M_{par} between the proposed AVFI topology, and the existing RSC and NSC converters under the buck–boost conversion.

$$C_i = \frac{m_{\text{qc},i}}{M_{\text{SSL}}} C_{\text{TOT}} \tag{19b}$$

$$M_{\text{par}} \triangleq \frac{1}{M_{\text{SSL}}} \sum_{i=1}^{n} \left[m_{\text{qc},i} \left(\frac{|\Delta V_{\text{CB},i}|}{V_{\text{IN}}} \right)^2 \right] \tag{19c}$$

where β denotes the ratio between the bottom-plate parasitic capacitance (C_{bot}) and C_{fly}. The C_i expression in (19b) results from the optimization for C_{fly} under the total area constrained condition, with M_{SSL} as defined in (13). Here, we define the topology-dependent parasitic loss factor M_{par} in (19c) for the performance comparison among different existing topologies. Fig. 10 gives a comparison of M_{par} for the proposed AVFI topology and the state-of-the-art RSC/NSC converters. It can be observed that the proposed AVFI topology achieves a significant reduction in M_{par} when compared with both the RSC and NSC, especially for large VCRs in boost mode.

D. Voltage Rating

The voltage rating of both capacitors and power switches are also important parameters to be considered for fully integrated SC converters. For simplicity, we consider only the boost conversion case. Similar consideration can also be readily applied to buck conversions. The conventional integer boost Dickson topologies have linearly increased capacitor voltage rating V_C which is maximally equal to $V_{\text{OUT}}-V_{\text{IN}}$. In contrast, V_C in integer boost SP topologies equal to V_{IN} for all power cells. Similar to the case of Dickson, in the proposed AVFI topology, the maximum required V_C is equal to $|V_{\text{OUT}}-V_{\text{IN}}|$ for VCR $\geq$ 2, and equal to V_{IN} for 1 $\leq$ VCR $\leq$ 2 in boost mode. Similarly, in buck mode, the maximum required V_C is equal to $|V_{\text{IN}}-V_{\text{OUT}}|$ when VCR $\leq$ 0.5, and equal to V_{OUT} when 0.5 $\leq$ VCR $\leq$ 1.

For power switch voltage rating V_R, in conventional integer boost Dickson converter, it is equal to $2V_{\text{IN}}$ for the switches on the top-plate side and V_{IN} for those on the bottom-plate side for all the power cells. In SP boost converter, both the top- and bottom-plate switches block linearly increased voltages along the power cells. The maximum V_R in the SP case is equal to $V_{\text{OUT}}-V_{\text{IN}}$ on both the top- and bottom-plate side. In the proposed AVFI topology, the maximum blocked voltage across the switches on the top-plate side is $|V_{\text{OUT}}-V_{\text{IN}}|$ both in buck and boost mode. For the bottom-plate side, the maximum V_R level is equal to V_{IN} and V_{OUT} in boost and buck mode, respectively.

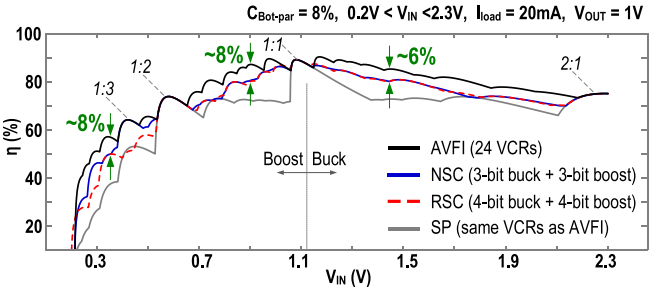


Fig. 11. Comprehensive simulation comparison between AVFI and the existing topologies over a wide input range.

In terms of boost conversion, when compared with the existing topologies (i.e., ladder, Dickson, and SP), ladder achieves the most relaxed blocking voltages for both C_{fly} and switches. However, the ladder has exponentially increased R_{SSL} which limits its application in on-chip implementations. In general, under the same VCRs, the proposed AVFI converter faces the same maximum C_{fly} blocking voltage as Dickson converter but with a higher switch blocking voltage requirement. The major limitation of Dickson topology is the inflexible VCR generation, which has been resolved in the AVFI converter. Compared with SP topology, the proposed AVFI realizes improved R_{SSL} and parasitic loss with a similar switch blocking voltage requirement. However, the SP topology has an advantage on the C_{fly} blocking voltage over both the proposed AVFI and Dickson converters.

E. System-Level Simulation

To demonstrate the effectiveness of the proposed AVFI topology, we performed simulations to provide quantitative comparisons with existing SP, RSC, and NSC topologies. Fig. 11 shows the system-level simulation accounting for all the losses. The input voltage range is from 0.2 to 2.3 V. The output voltage was regulated to 1 V while delivering a loading current of 20 mA assuming the same total capacitance. C_{bot} is set to 8% of C_{fly}. The total number of buck–boost VCR is 24 for the proposed converter. In addition, all the AVFI/RSC/NSC topologies have an identical structure under specific ratios (i.e., 2:1, 1:1, 1:2, and 1:3). Across the entire conversion range, the proposed AVFI converter achieves improved overall efficiency of up to 8% when compared with RSC and NSC designs.

IV. AVFI Design Procedures

This section demonstrates the design procedures of the proposed AVFI topology generation method followed by the 7:4 buck and 3:8 boost examples. The operation characteristics of the proposed AVFI topology will be illustrated to reveal the power stage implementation insights as well as the intuitive interpretations of the achieved lower parasitic loss mechanism.

The proposed method can generate a specific topology with any arbitrary VCR, and Fig. 12 summarizes its detailed steps, where we present a few design examples using buck–boost VCRs. For a given rational VCR, the total number of required power cells can be directly observed according to the linear

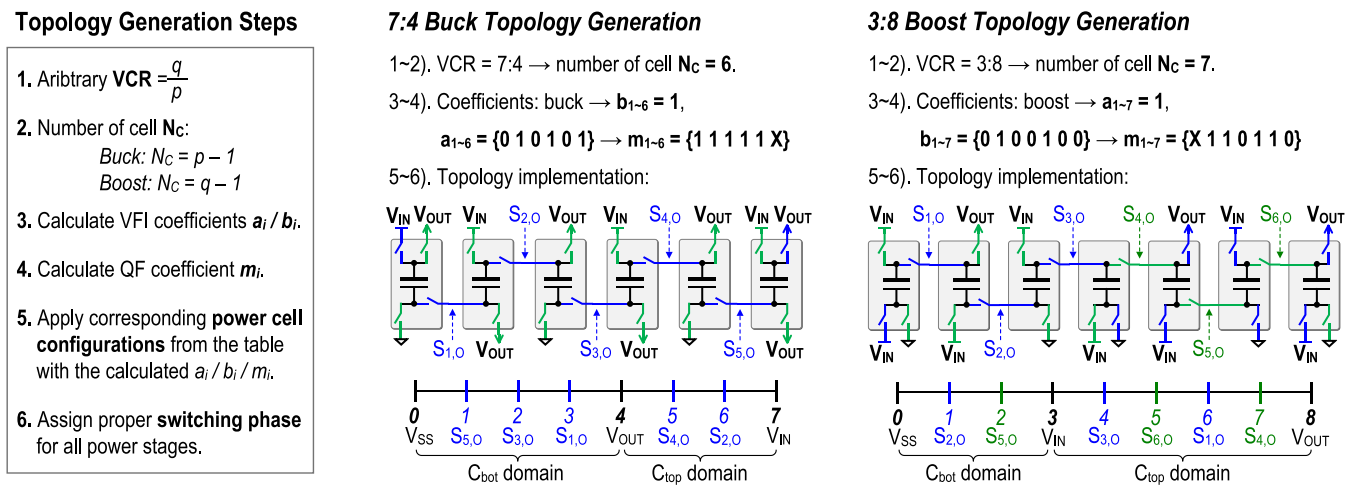


Fig. 12. VCR driven design flow and the corresponding examples for the buck–boost conversion using the proposed AVFI topology generation method.

topology feature discussed in Section II-A. The corresponding topology parameters a_i and b_i can be calculated iteratively through (9) and (10). Based on the obtained a_i and b_i, we can have a corresponding set of m_i by (11) and (12) for power cell selection using the cell summary table of Fig. 2. The last step is to assign the switching phases in each cell.

In both examples for the buck and boost rational VCR generation (Fig. 12), each power stage generates equally distributed voltage levels from V_{SS} to the highest level of the conversion domain (i.e., V_{IN} in buck mode and V_{OUT} in boost mode) similar to the patterns of linear topologies of Figs. 1 and 3. Each level step is equal to $1/(n+1)$ in both $(n+1)$:x buck and x:$(n+1)$ boost conversions. The generated levels can be divided into two voltage distribution domains based on the C_{top} and C_{bot}, as illustrated in Fig. 12. During buck mode operation, C_{bot} processes voltage levels within $[V_{SS}, V_{OUT}]$, while C_{top} converts voltage levels within $[V_{OUT}, V_{IN}]$. Similarly, in boost conversion, C_{top} operates within $[V_{IN}, V_{OUT}]$ and C_{bot} within $[V_{SS}, V_{IN}]$. In addition, the C_{top} domain is always higher than the C_{bot}. This bounded domain property can well define the required power switch voltage stress and the corresponding driving rails, which is also exploited in the power cell design of Section V-C and the RSBD implementation of Section V-D, respectively.

Another observation is that the charge transfer between all adjacent cells exhibits the C_{top}-to-C_{top} and C_{bot}-to-C_{bot} phenomena. And, such patterns also appear in the lower ΔV_{CB} selection of Fig. 6 when deriving the m_i algorithm. In fact, this pattern universally exists in all generated AVFI topologies by the proposed method (similar to Dickson converters). Together with the previously discussed C_{top}/C_{bot} domain property, it intuitively explains the lower ΔV_{CB} characteristic for the proposed AVFI topology. Specifically, since the top-plate voltage V_{Ctop} is always higher than the bottom-plate voltage V_{Cbot}, cell interfacing between the same capacitor plates (i.e., C_{top}-to-C_{top} and C_{bot}-to-C_{bot}) will definitely achieve lower ΔV_{CB} in the cell switching when compared with the opposite (i.e., C_{top}-to-C_{bot} and C_{bot}-to-C_{top}).

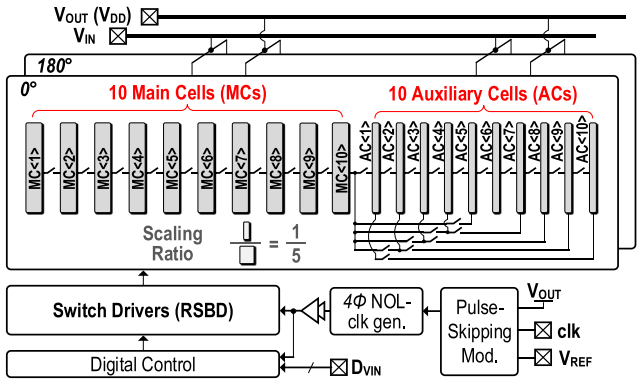


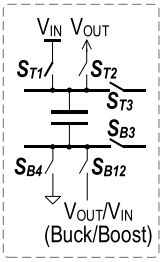
Fig. 13. Overview of the implemented SC converter with 24 rational buck–boost VCRs using 10 MC + 10 AC partitionable power stage.

V. Converter Design and Implementation

The previous discussion introduces design examples for single rational VCR implementation. Here, we present the complete design and implementation of a fully integrated SCPC with buck–boost FVCRs supporting a wide input voltage range. The design tackles the challenge of full power cell utilization and efficient power switch driving to enhance on-chip power density and reduce the switching loss.

A. Converter Overview

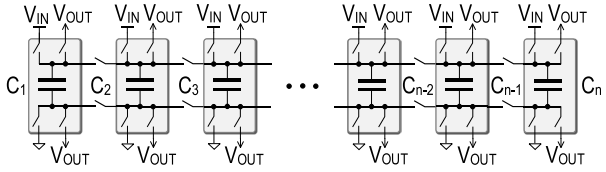
A reconfigurable SCPC was implemented based on the proposed AVFI topology with 24 rational buck–boost VCRs (11 buck + 13 boost) covering a conversion range from 2:1 to 1:7, as illustrated in Fig. 13. The 10 MCs + 10 ACs partitionable power stage can theoretically generate a total of 79 buck–boost VCRs (including 1:1), among which we implemented a subset of 24 with reference to the target conversion range and power level. The designed converter operates in dual-branch interleaving with the four-phase non-overlapping clock signal generated through an injected master clock to eliminate both the shoot through and reversion



Switch	$a_i m_i$ (Buck)				$b_i m_i$ (Boost)			
	00	01	10	11	00	01	10	11
S_{T1}	off	off	en	en	off	en	en	off
S_{T2}	off	en	en	off	off	off	en	en
S_{T3}	en	off	off	en	en	en	off	off
S_{B12}	en	off	off	en	en	off	off	en
S_{B3}	off	en	en	off	off	off	en	en
S_{B4}	en	en	off	off	en	en	off	off

*Special case: S_{T1} in first stage & S_{T2} in last stage are always enabled.

(a)



(b)

Fig. 14. (a) Rational power cell and the corresponding switch control table (*en*: enable). (b) Generalized $(n+1)$:x topology framework implementation.

losses [41], [42]. The digital controller serves to update the converter VCR based on the external 5-bit digital signal ($D_{\mathrm{VIN\_S}}$), as well as to regulate the output loading based on hysteretic pulse-skipping modulation.

B. Partitionable Power Stage Design

According to the derived VCR expression in (7), the proposed topology framework features programmable VCR with a fixed number of cells. To accommodate the difference in parameter settings for various VCRs, a general rational power cell structure, shown in Fig. 14(a), was also proposed. Referring to the switch control summary table, it can be reconfigured into any cell type among the eight DSC and QFC structures of Fig. 2. This facilitates practical implementation using the proposed AVFI framework, where any rational ratios can be realized by cascading rational power cells. Fig. 14(b) shows a buck $(n+1)$:x example based on the AVFI framework using the rational cell in Fig. 14(a).

The topology framework for the implemented VCRs consists of $(n+1)$:x and x:$(n+1)$ conversions with $x \leq n$, where $n = \{1, 2, 3, 4, 5, 6, 10\}$. Here, the VCRs are chosen based on the implementation complexity and the induced efficiency improvement. The unit charge-flow property of the proposed AVFI topology enables the use of identical power cells which can significantly simplify the multi-VCR implementation. However, to achieve full capacitance utilization for all the targeted VCRs, the conventional brute force method requires a total of 60 unit power cells which inevitably increases the implementation complexity. To resolve this problem, we designed a partitionable power stage architecture consisting of 10 MCs and 10 ACs with a sizing ratio of 5 (Fig. 13). The 10 ACs can either work as 10 individual small cells in parallel with the 10 MCs for $n = \{1, 5, 10\}$, or be grouped as two large cells to serve as two MCs for $n = \{2, 3, 4, 6\}$. We implement both the MCs and ACs using the modular rational cell structure from Fig. 14(a). Fig. 15 outlines the corresponding partitioning modes for implementing the targeted 24 VCRs. The connecting wires at the bottom of the

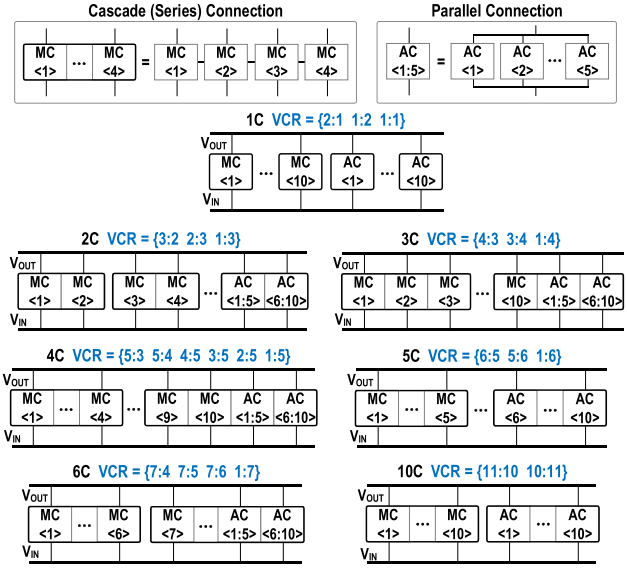


Fig. 15. Summary of the seven operation modes for the partitionable power stage to implement the targeted 24 VCRs.

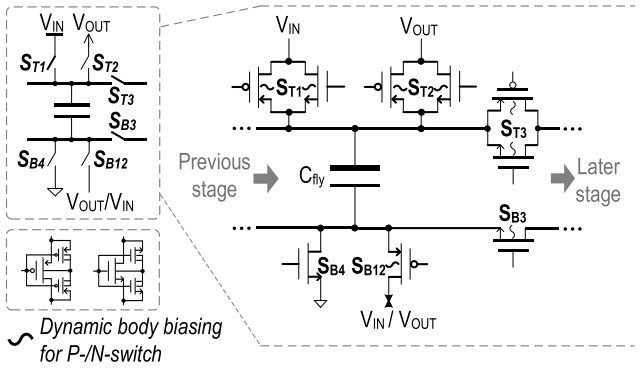


Fig. 16. Power cell implementation.

ACs in Fig. 13 show the reconfigurability of all the 10 ACs to achieve full capacitor utilization at different VCRs in Fig. 15, where the ACs can be rearranged into either series or parallel configurations. With the proposed partitionable power stage architecture, the total number of cells can be reduced to 20, leading to a threefold improvement when compared with the conventional method.

C. Power Cell Implementation

Fig. 16 illustrates the implementation of the rational power cell in Fig. 14(a), together with the schematic of the dynamic body biasing N-/P-switch. Each cell contains six power switches, with $S_{T1,T2,T3}$ and $S_{B12,B3,B4}$ connected to C_{top} and C_{bot} of the flying capacitor, respectively. Except for S_{B4}, all the other switches employ a DTMOS-based dynamic body biasing technique [43] to enhance switch conductance while ensuring proper biasing of substrate junction diodes. S_{T1-3} adopt P/N complementary switches that are alternately activated in buck–boost modes to relax the possible voltage stress induced in their driver circuits, to be discussed next. The target V_{OUT} is around 1 V. Together with the well-bounded bottom-plate voltage domains in both the buck (from V_{IN} to V_{SS}) and boost (from V_{OUT} to V_{SS}) modes,

States (for T_3)		Buck ⇨ $V_{IN} > V_{OUT}$ (V_{DD}) (en = 1, Iv = 0)	Boost ⇨ $V_{IN} < V_{OUT}$ (V_{DD}) (en = 1, Iv = 1)	Disable (en = 0)
Φ_1	S_P	$V_{GP,on} = V_{pass} - V_{DD}$	$V_{GP,off} = V_{DD}$	(buck) $V_{GP,dis} = V_{IN}$ $V_{GN,dis} = V_{DD}$
	S_N	$V_{GN,off} = V_{DD}$	$V_{GN,on} = V_{pass} + V_{DD}$	
Φ_2	S_P	$V_{GP,off} = \begin{cases} V_n & \text{if } V_n > V_{n+1} \\ V_{n+1} & \text{if } V_{n+1} > V_n \end{cases}$	$V_{GP,off} = V_{DD}$	(boost) $V_{GP,dis} = V_{DD}$ $V_{GN,dis} = V_{SS}$
	S_N	$V_{GN,off} = V_{DD}$	$V_{GN,off} = \begin{cases} V_n & \text{if } V_n < V_{n+1} \\ V_{n+1} & \text{if } V_{n+1} < V_n \end{cases}$	
		$V_{DD} < V_{pass} < V_{IN}$	$V_{IN} < V_{pass} < V_{DD}$	–

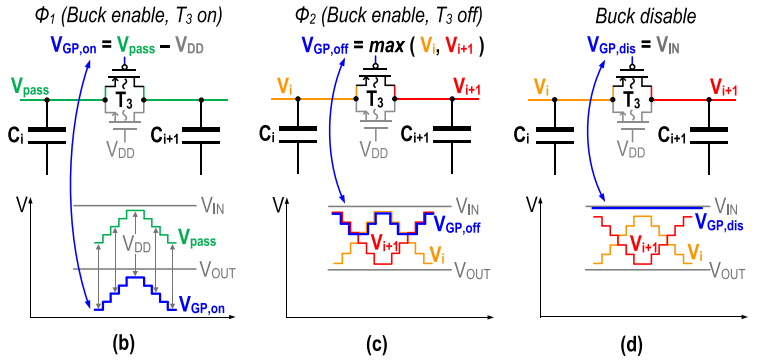


Fig. 17. Three-state switch operation illustrations of the adaptive gate driving for the P-switch in S_{T3} under buck conversion. (a) Complete summary for all the possible operations. (b) Switch-on. (c) Switch-off. (d) Disable.

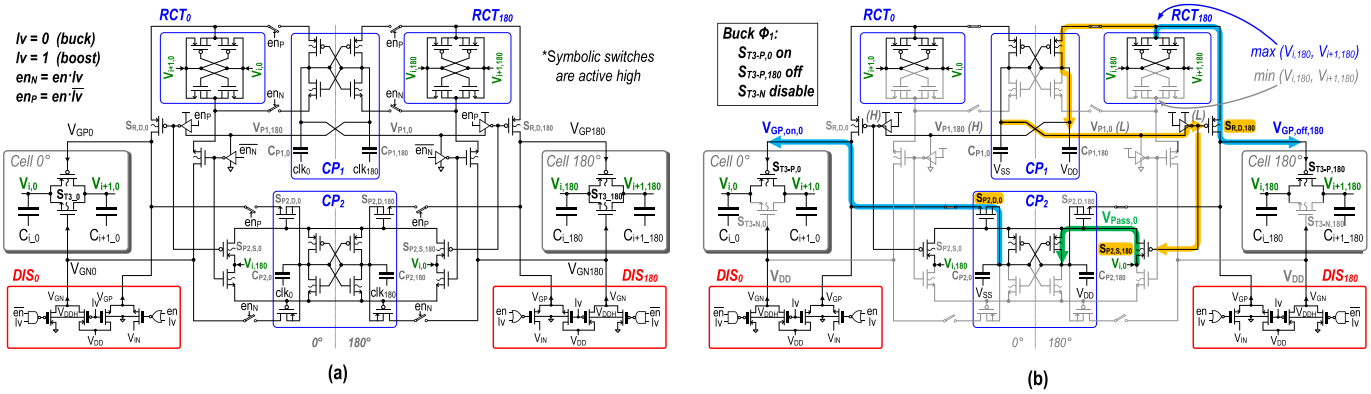


Fig. 18. (a) Circuit implementation of the proposed RSBD for S_{T3} and (b) its operating status in buck conversion mode.

these conditions enable the use of low-voltage transistors for all power switches of S_{B12}, S_{B3}, and S_{B4}, effectively reducing the driving loss especially in heavy load conditions. Because of the targeted V_{IN} range, a similar principle can be applied to employ low-voltage switches on the top-plate side.

The top-plate switches $S_{T1,T2,T3}$ have three operating states, including two enable states for P-switch and N-switch in the buck and boost modes, respectively, and one disable state in which both P-/N-switches are turned off. As an example, Fig. 17(a) tabulates the three-state adaptive driving behaviors for S_{T3}. The dual-phase operations, represented as Φ_1 and Φ_2, correspond to the switch-on and -off conditions, respectively. Fig. 17(b)–(d) displays the exact three-state gate driving behaviors for S_{T3} in buck mode. Accordingly, the lowest potential on C_{top} should be V_{OUT}, which is also the supply V_{DD} of the RSBD control circuit. For buck conversions, the N-switch of S_{T3} is kept disabled by tying its gate terminal to V_{DD}. The use of P-switch instead of N-switch can prevent possible device over-stressing in the RSBD control block without using stacking devices.

D. Proposed RSBD

The bootstrapping technique is generally implemented to enforce the switch gate–source voltage (V_{GS}) to maintain a low on-resistance. Among the six power switches, S_{T3} and S_{B3} which connect C_{top} and C_{bot} of adjacent power stages exhibit the most driving challenge due to the wide terminal voltage dynamics under different VCRs. The generated gate driving signal should accommodate the higher/lower potential side across the switch accordingly.

Fig. 18(a) shows the RSBD circuit implementation. To ensure proper driving rail selection for all the three operation states, the proposed RSBD is realized by four active function blocks (CP_1, CP_2, RCT_0, and RCT_{180}) and two disable blocks ($DIS_{0/180}$). All the active function blocks operate in two active buck–boost operation states to realize adaptive reference voltage selection and power switch driving control. $DIS_{0/180}$ serves to properly turn off the power switch in the disable state, during which all the four active function blocks are also shut down. As mentioned in Section V-C, the use of P/N power switches for $S_{T1,T2,T3}$ reduces the voltage stress on the state control circuits in Fig. 18. Specifically, if using only N-switch, all the symbolic switches, and logic cells as well as the disable function blocks should sustain a voltage stress about three times of V_{DD} during the switch-on driving state of the RSBD. In that case, even the high-voltage transistor available in typical bulk CMOS process (generally with ~2 V_{DD} voltage stress tolerance) cannot fulfill the requirement. Even though this issue can be resolved by transistor stacking, it will inevitably increase the internal switching loss in the RSBD. Notice that although the exact implementation and optimization is design and technology specific, the proposed RSBD technique can still be generally applied with appropriate modification accordingly.

Due to the fully differential implementation, the proposed RSBD circuit is also applicable to multiple-branch interleaving

converters with an even number of interleaved branches. The RSBD is controlled through external signals *en* and *lv* to generate internal controls for switch enabling and mode selection. As an example, the three-state driving operations for the P-switch in S_{T3} using the RSBD sub-building blocks are detailed as follows.

1) Charge Pump CP_2 for Switch-on Driving: The driving signal $V_{\mathrm{GP,on,0}}$ should be delivered to the 0° power branch in Φ_1 to turn on the power switch S_{T3-P} as illustrated in Fig. 17. During this phase, the gate voltage of S_{T3-P} should be maintained as $V_{\mathrm{GP,on,0}} = V_{\mathrm{pass}}-V_{\mathrm{DD}}$, where V_{pass} is the top-plate pass voltage on both C_i and C_{i+1}. The targeted control signal is generated by the sub-building block CP_2, which is essentially a bi-directional charge pump circuit with cross-coupled sampling and pumping switches, as shown in Fig. 18(b). The clock signals (i.e., clk_0 and clk_{180}) are switching between V_{SS} and V_{DD}. $C_{P2,0}$ generates the voltage $V_{\mathrm{GP,on,0}}$ to turn on $S_{T3-P,0}$ on the 0° side. Meanwhile, $C_{P2,180}$ samples the $V_{\mathrm{pass,0}}$ from the 0° branch for generating $V_{\mathrm{GP,on,180}}$ in the next clock phase. Furthermore, the V_{pass} sampling control is internally generated by P_1. Referring to Fig. 18(b), the generated signal from CP_1 turns on $S_{P2,S,180}$ in order that $V_{\mathrm{pass,0}}$ can be sampled on $C_{P2,180}$. At the same time, $S_{P2,D,0}$ is turned on (as $V_{\mathrm{pass,0}}-V_{\mathrm{GP,on,0}} = V_{\mathrm{DD}}$), connecting $C_{P2,0}$ to $S_{T3-P,0}$ with the control voltage $V_{\mathrm{GP,on,0}}$.

Noteworthy, the charge sharing between C_{P2} and the gate terminal of the power switch can lead to a reduction of the driving voltage from the desired level. Considering the tradeoff between the driving level degradation and driver area overhead, we select the capacitance of C_{P2} as approximately six times the corresponding gate capacitance to ensure the effective driving voltage above 85% of the desired level.

2) Charge Pump CP_1 for Internal Control: Similar to CP_2, the sub-building block CP_1 is also a bi-directional charge pump but for the RSBD internal control. During Φ_1, $C_{P1,0}$ pumps out the internal control voltage $V_{P1,0}$ to turn on $S_{P2,S,180}$, passing V_{pass} from the 0° branch to charge $C_{P2,180}$. It also turns on $S_{R,D,180}$ to deliver the switch-off control signal $V_{\mathrm{GP,off,180}}$ to $S_{T3-P,180}$ on the 180° side, where RCT_{180} generates $V_{\mathrm{GP,off,180}}$. Simultaneously, $C_{P1,180}$ samples $V_{\mathrm{GP,off,180}}$ to generate the equivalent internal control in the next clock phase. In Φ_1, $V_{P1,180}$ turns off $S_{R,D,0}$ and $S_{P2,S,0}$ to isolate the 0° power cell from both RCT_0 and the 180° power cell. Since the control switches inside the RSBD are much smaller than the power switches, C_{P1} was set to 1/3 of C_{P2}.

3) Rectifier $\mathrm{RCT}_{0/180}$ for Reference Selection: Both RCT_0 and RCT_{180} provide adaptive reference selection across the power switch, with the two PMOS and NMOS transistors selecting the higher and lower levels between the two terminals across a power switch, respectively. The control signals en_N and en_P, shown in Fig. 18(a), serve to pass the selected higher and lower levels, which are utilized in the buck and boost modes, respectively. As illustrated in Fig. 17(c), turning off S_{T3-P} requires connecting its gate terminal to the higher potential side. In this case, the higher level selection circuit of RCT_{180} generates the required signal $V_{\mathrm{GP,off,180}}$, which passes through switch $S_{R,D,180}$ and then drives $S_{T3-P,180}$. Since $S_{T3-P,0}$ is turned on, RCT_0 has no effect in this phase.

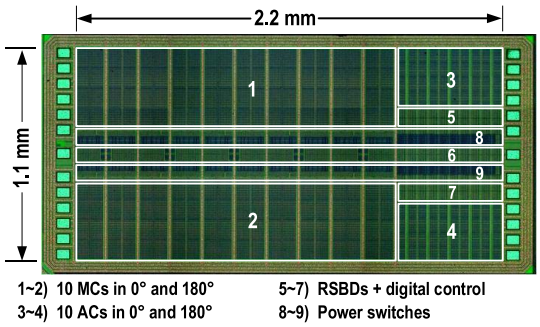


Fig. 19. Annotated chip micrograph of the converter prototype.

In this paper, the worst case voltage difference in the reference selection circuit is ideally 0.44 V, which is mainly limited by the minimum V_{IN} of 0.22 V. From simulation, it can be concluded that in the worst case (1:7 conversion) the $\mathrm{RCT}_{0/180}$ block will induce a finite settling error, and the resultant loss is negligible when compared with the other converter losses.

4) Disable Blocks $DIS_{0/180}$: Referring to Fig. 17(d), when S_{T3-P} is disabled, the gate voltage $V_{\mathrm{GP,dis}}$ should be connected to the highest top-plate potential (i.e., V_{IN} in buck mode) to ensure proper switch-off operation. The disable function (determined by *en* and *lv*) is executed by the two disable blocks [Fig. 18(b)] for the 0° and 180° branches. During the disable state, the disable circuits connect the P-switch gates to the highest top-plate voltage (i.e., V_{IN} in buck mode and V_{OUT} in boost mode). Similarly, they also connect the N-switch gates to the lowest top-plate voltage (i.e., V_{DD} in buck and V_{SS} in boost).

VI. Chip Implementation and Measurement

The proposed AVFI converter with 24 VCRs was realized in 65-nm bulk CMOS, occupying an active area of 2.42 mm^2. Fig. 19 shows the annotated chip micrograph. We placed the RSBDs and digital control in the center for dual branch power cell control with 10 MCs and 10 ACs on the two sides. All the flying capacitors employed vertical stacking of thin-oxide MOS capacitors together with MIM capacitors (2 $\mathrm{fF}/\mu\mathrm{m}^2$), resulting in a capacitance density of $\sim$10 $\mathrm{fF}/\mu\mathrm{m}^2$ (depending on the MOS capacitor biasing condition). The on-chip C_{fly} and output filtering capacitor C_{OUT} are 8 and 6 nF, respectively, where C_{OUT} is distributed in each cell. The chip prototype supports an input conversion range from 0.22 to 2.4 V, with a regulated output between 0.85 and 1.2 V. The reference voltage V_{REF} for V_{OUT} regulation was supplied externally. With an external clock frequency of 25 MHz, load regulation is accomplished using pulse-skipping modulation, with a target output power level of $>$20 mW using a resistive load.

A. Conversion Efficiency

Fig. 20 shows the measured conversion efficiency over different input voltage ranges. The measured peak power conversion efficiency (η_{peak}) is 84.1% for both $V_{\mathrm{OUT}} = 1$ and 1.2 V. At $V_{\mathrm{OUT}} = 0.85$ V, the measured η_{peak} is 83.8%.

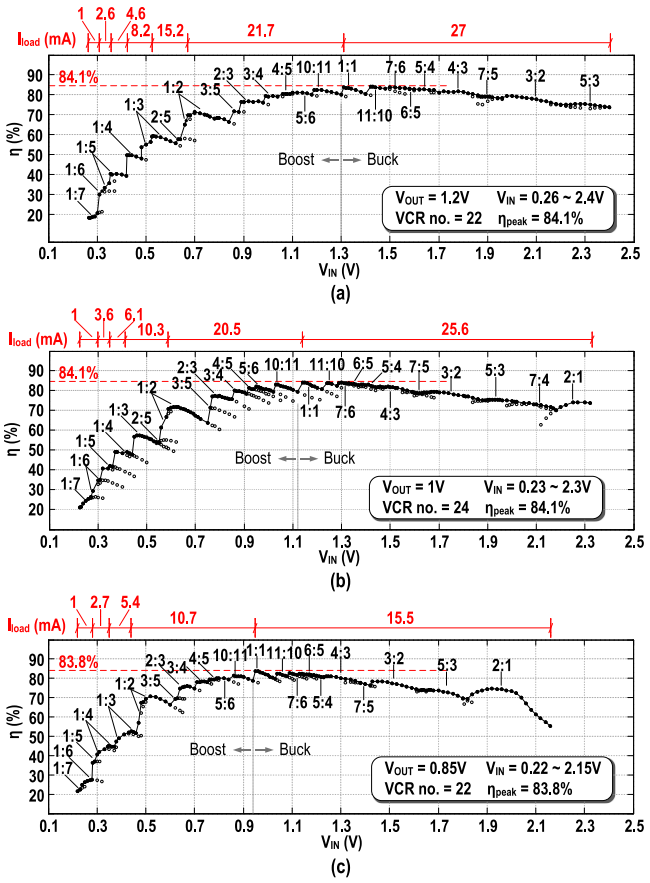


Fig. 20. Measured power conversion efficiency over the entire V_{IN} range and regulated at different V_{OUT} levels.

The corresponding output power densities are 13.4, 10.6, and 5.4 mW/mm^2 at V_{OUT} = 1, 1.2, and 0.85 V, respectively. A drop in η_{peak} can be observed at high VCRs in boost mode due to the exponential increase in R_{SSL}. Apart from that the power loss from the regulation control blocks is also becoming more significant due to the lower output current at high VCRs. The peak efficiency occurs at around unity VCRs due to the lower parasitic loss. It can also be observed that not all VCRs can contribute to an efficiency improvement at high output power as limited by the high M_{SSL} and M_{FSL}. For instance, the M_{SSL} and M_{FSL} for 7:4 are higher than that of 5:3 with reference to Figs. 8 and 9. However, both have similar M_{par} as shown in Fig. 10. Consequently, the VCR of 7:4 only covers a limited conversion range at $V_{OUT} = 1$ V in Fig. 20(b) but achieves lower efficiency than that of 5:3 at $V_{OUT} = 0.85$ V in Fig. 20(c). The same argument applies to the absence of ratio 2:5 in Fig. 20(c).

B. Power Range

Fig. 21 displays the measured output power range versus efficiency for each VCR at V_{OUT} = 1 V, with distinct load driving ability due to the difference in power stage loss under different VCRs. The maximum output power is up to 82 mW at 2:1, which exhibits the lowest R_{SSL}. This corresponds to a power density of 33.9 mW/mm^2 at 74.5% efficiency. In addition, all the buck configurations can deliver an output power of more than 30 mW thanks to the bounded

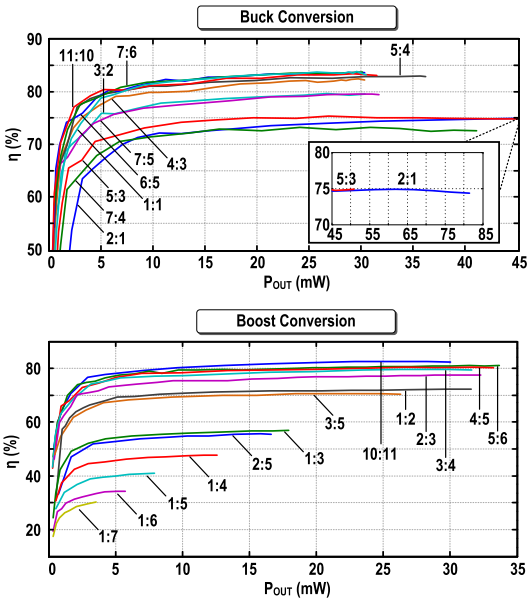


Fig. 21. Measured output power range versus conversion efficiency for all the implemented VCRs under $V_{OUT} = 1$ V.

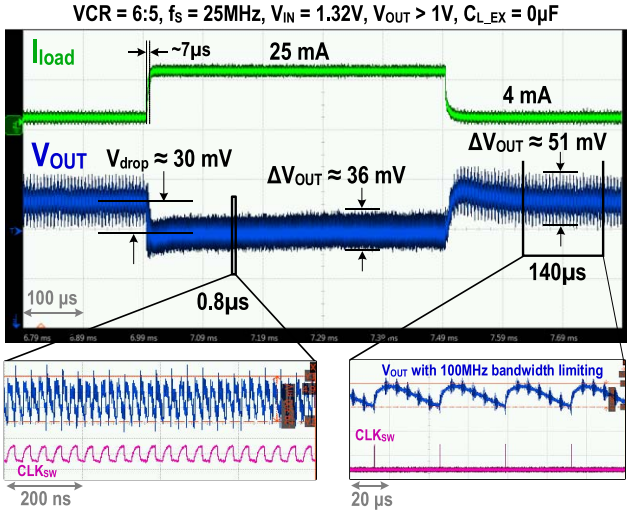


Fig. 22. Measured output waveforms without external filtering capacitor C_L.

M_{SSL} according to (6). On the contrary, the boost VCR configurations show a reduced driving capability as a result of the exponentially increased M_{SSL}. For all the boost VCRs not more than 1:2 (except from 3:5 whose M_{SSL} is relatively higher), the proposed converter can still deliver a loading power level of >30 mW.

C. Output Transient

Fig. 22 depicts the measured output waveforms with a stepped loading current (I_{load}) between 4 and 25 mA at 6:5 and V_{OUT} = 1 V using pulse-skipping modulation at 25 MHz (CLK_{SW}). The step response of 5 μs is mainly limited by the measurement setup. It should be noted that a higher output voltage transient droop is expected if a faster step is applied to the system. The corresponding ΔV_{OUT} is around 51 mV when $I_{load} = 4$ mA with no external output filtering capacitor. Further reduction in output ripple can be achieved by increasing the number of interleaving branches.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART WORKS

	This work ISSCC'18 [39]	D. Lutz ISSCC'16 [33]	C. K. Teh ISSCC'16 [28]	M. Saadat ASSCC'15	X. Hua CICC'15	Y. Lin ESSCIRC'17	J. Jiang JSSC'17 [30]
Technology	**65nm CMOS**	0.35µm HVCMOS	65nm CMOS	0.25µm CMOS	65nm CMOS	0.25µm CMOS	130nm CMOS
Converter Type	**Buck-Boost**	Buck-Boost	Buck-Boost	Buck-Boost	Buck-Boost	Buck only	Buck only
Number of VCR	**11 buck + 13 boost**	8 buck + 9 boost	5 buck + 1 boost	4 buck + 4 boost	3 buck + 3 boost	187 buck	6 buck
Integrated C_{fly}	**MOS + MIM**	MIM	MOS + External	MIM	N/A	N/A	External
V_{IN} Range [V]	**0.22 to 2.4**	2 to 13	0.85 to 3.6	0.6 to 2.4	0.5 to 3.3	3.3	1.6 to 3.3
V_{OUT} [V]	**0.85 to 1.2**	5	0.1 to 1.9	1.2 to 1.5	1	0.4 to 2.8	0.5 to 3
I_{OUT_MAX} [mA]	**80.1**	4	10	0.1	0.0033	10	120
η_{peak} [%]	**Buck: 84.1# Boost: 83.2#**	Buck: 81.5 Boost: 70.9	Buck: 95.8 Boost: 90.5	76	70.4	87	91
Power Density @ η_{peak} [mW/mm^2]	**Buck: 13.4# Boost: 10.8#**	*Buck: 0.96 *Boost: 0.15	N/A	*0.062	*0.0069	*1	N/A

*Estimated from the reported measurement results.
#Power from external sources such as external clock and voltage reference are not included.

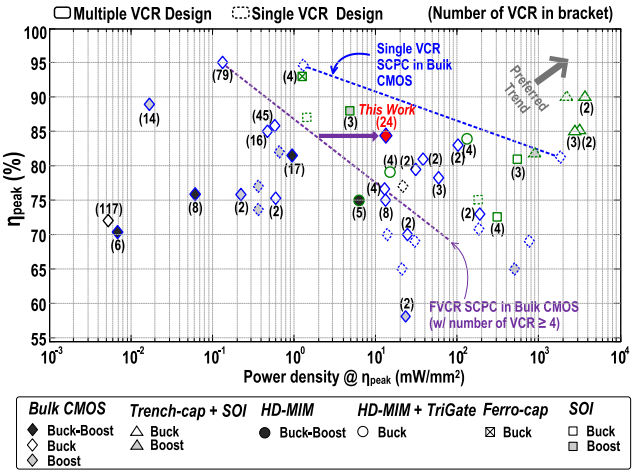


Fig. 23. Performance benchmarking with state-of-the-art fully integrated SC converters in bulk CMOS and other special processes.

D. Performance Comparison and Benchmarking

Table I outlines the measured performance of the proposed SCPC. This paper accomplishes the highest number of VCRs among existing buck–boost designs. As the AVFI topology intrinsically features lower parasitic loss than existing works, a high power density up to 13.4 mW/mm^2 and a high peak efficiency of 84.1% are concurrently achieved using the MOS+MIM capacitors. When compared with the state-of-the-art recursive buck–boost SCPC in [33], this paper implements an increased number of VCRs and a higher peak efficiency, as well as an improved power density by $>13\times$.

Fig. 23 shows the benchmarking for state-of-the-art fully integrated SC dc–dc converters, classifying designs with single (solid markers) and multiple (dashed markers) VCRs. It can be observed that the power density generally becomes lower as the number of VCR increases. For fair comparisons, Fig. 23 shows the comparison of this paper with other FVCR designs in bulk CMOS (with number of VCR ≥ 4). It can be concluded that this design achieves a significant power density improvement except for those using special processes.

VII. CONCLUSION

This paper proposed a systematic SCPC topology design technique featuring fine-grained rational buck–boost VCR generation with optimal R_{SSL}, R_{FSL}, and C_{bot} parasitic loss in contrast to existing methods. A partitionable power stage architecture that consists of main and auxiliary power cells was introduced to significantly reduce implementation complexity with full capacitor utilization. Effective power switch-on/-off operation over wide voltage dynamics was guaranteed by the proposed RSBD. A fully integrated buck–boost SCPC with 24 rational VCRs was implemented in a standard 65-nm bulk CMOS process, attaining 13.4 mW/mm^2 on-chip power density at a peak conversion efficiency of 84.1%, which is the state of the art among existing fully integrated FVCR SC converter designs without using special processes.

REFERENCES

[1] G. Villar-Piqué, H. J. Bergveld, and E. Alarcón, "Survey and benchmark of fully integrated switching power converters: Switched-capacitor versus inductive approach," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4156–4167, Sep. 2013.
[2] S. R. Sanders, E. Alon, H.-P. Le, M. D. Seeman, M. John, and V. W. Ng, "The road to fully integrated DC–DC conversion via the switched-capacitor approach," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4146–4155, Sep. 2013.
[3] M. Steyaert, T. Van Breussegem, H. Meyvaert, P. Callemeyn, and M. Wens, "DC-DC converters: From discrete towards fully integrated CMOS," in *Proc. IEEE ESSDERC*, Sep. 2011, pp. 42–49.
[4] M. Steyaert, F. Tavernier, H. Meyvaert, A. Sarafianos, and N. Butzen, "When hardware is free, power is expensive! Is integrated power management the solution?" in *Proc. IEEE ESSCIRC*, Sep. 2015, pp. 26–34.
[5] J. Li, J.-S. Seo, I. Kymissis, and M. Seok, "Triple-mode, hybrid-storage, energy harvesting power management unit: Achieving high efficiency against harvesting and load power variabilities," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2550–2562, Oct. 2017.
[6] X. Wu *et al.*, "A 20-pW discontinuous switched-capacitor energy harvester for smart sensor applications," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 972–984, Apr. 2017.

[7] X. Liu, L. Huang, K. Ravichandran, and E. Sánchez-Sinencio, "A highly efficient reconfigurable charge pump energy harvester with wide harvesting range and two-dimensional MPPT for Internet of Things," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1302–1312, May 2016.

[8] T. Ozaki, T. Hirose, H. Asano, N. Kuroki, and M. Numa, "Fully-integrated high-conversion-ratio dual-output voltage boost converter with MPPT for low-voltage energy harvesting," *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2398–2407, Oct. 2016.

[9] M. Alioto, E. Consoli, and M. J. Rabaey, "EChO reconfigurable power management unit for energy reduction in sleep-active transitions," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1921–1932, Aug. 2013.

[10] N. Butzen and M. S. J. Steyaert, "Scalable parasitic charge redistribution: Design of high-efficiency fully integrated switched-capacitor DC-DC converters," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2843–2853, Dec. 2016.

[11] N. Butzen and M. S. J. Steyaert, "Design of soft-charging switched-capacitor DC–DC converters using stage outphasing and multiphase soft-charging," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3132–3141, Dec. 2017.

[12] H. Meyvaert, G. V. Piqué, R. Karadi, H. J. Bergveld, and M. S. J. Steyaert, "A light-load-efficient 11/1 switched-capacitor DC-DC converter with 94.7% efficiency while delivering 100 mW at 3.3 V," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2849–2860, Dec. 2015.

[13] H. Meyvaert, T. Van Breussegem, and M. Steyaert, "A 1.65 W fully integrated 90 nm bulk CMOS capacitive DC-DC converter with intrinsic charge recycling," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4327–4334, Sep. 2013.

[14] T. M. Andersen *et al.*, "A sub-ns response on-chip switched-capacitorDC-DC voltage regulator delivering 3.7W/mm^2 at 90% efficiency usingdeep-trench capacitors in 32 nm SOI CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 90–91.

[15] G. V. Piqué, "A 41-phase switched-capacitor power converter with 3.8 mV output ripple and 81% efficiency in baseline 90 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 98–99.

[16] D. El-Damak, S. Bandyopadhyay, and A. P. Chandrakasan, "A 93% efficiency reconfigurable switched-capacitor DC-DC converter using on-chip ferroelectric capacitors," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers.*, Feb. 2013, pp. 374–375.

[17] R. Jain *et al.*, "A 0.45–1 V fully-integrated distributed switched capacitor DC-DC converter with high density MIM capacitor in 22 nm tri-gate CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 917–927, Apr. 2014.

[18] R. Jain, S. T. Kim, V. Vaidya, K. Ravichandran, J. W. Tschanz, and V. De, "Conductance modulation techniques in switched-capacitor DC-DC converter for maximum-efficiency tracking and ripple mitigation in 22 nm tri-gate CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1809–1819, Aug. 2015.

[19] S. T. Kim *et al.*, "Enabling wide autonomous DVFS in a 22 nm graphics execution core using a digitally controlled fully integrated voltage regulator," *IEEE J. Solid-State Circuits*, vol. 51, no. 1, pp. 18–30, Jan. 2016.

[20] B. Zimmer *et al.*, "A RISC-V vector processor with simultaneous-switching switched-capacitor DC-DC converters in 28 nm FDSOI," *IEEE J. Solid-State Circuits*, vol. 51, no. 4, pp. 930–942, Apr. 2016.

[21] X. Zhang and H. Lee, "A reconfigurable 2×/2.5×/3×/4× SC DC-DC regulator for enhancing area and power efficiencies in transcutaneous power transmission," in *Proc. IEEE CICC*, Sep. 2011, pp. 1–4.

[22] Y. K. Ramadass and A. P. Chandrakasan, "Voltage scalable switched capacitor DC-DC converter for ultra-low-power on-chip applications," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2007, pp. 2353–2359.

[23] H.-P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor DC-DC converters," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, Sep. 2011.

[24] G. V. Piqué, H. J. Bergveld, and R. Karadi, "A 1W 8-ratio switched-capacitor boost power converter in 140 nm CMOS with 94.5% efficiency, 0.5 mm thickness and 8.1 mm^2 PCB area," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2015, pp. 338–339.

[25] I. Vaisband, M. Saadat, and B. Murmann, "A closed-loop reconfigurable switched-capacitor DC-DC converter for sub-mW energy harvesting applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 2, pp. 385–394, Feb. 2015.

[26] A. Sarafianos and M. Steyaert, "Fully integrated wide input voltage range capacitive DC-DC converters: The folding Dickson converter," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1560–1570, Jul. 2015.

[27] A. Biswas, Y. Sinangil, and A. P. Chandrakasan, "A 28 nm FDSOI integrated reconfigurable switched-capacitor based step-up dc-dc converter with 88% peak efficiency," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1540–1549, Jul. 2015.

[28] C. K. Teh and A. Suzuki, "A 2-output step-up/step-down switched-capacitor DC-DC converter with 95.8% peak efficiency and 0.85-to-3.6 V input voltage range," in *ISSCC Dig. Tech. Papers*, Feb. 2016, pp. 222–223.

[29] Y. Lu, J. Jiang, and W.-H. Ki, "A multiphase switched-capacitor DC–DC converter ring with fast transient response and small ripple," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 579–591, Feb. 2017.

[30] J. Jiang, W.-H. Ki, and Y. Lu, "Digital 2-/3-phase switched-capacitor converter with ripple reduction and efficiency improvement," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1836–1848, Jul. 2017.

[31] S. Bang, A. Wang, B. Giridhar, D. Blaauw, and D. Sylvester, "A fully integrated successive-approximation switched-capacitor DC-DC converter with 31 mV output voltage resolution," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 370–371.

[32] L. G. Salem and P. P. Mercier, "A recursive switched capacitor DC-DC converter achieving $2^N - 1$ ratios with high efficiency over a wide output voltage range," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2773–2787, Dec. 2014.

[33] D. Lutz, P. Renz, and B. Wicht, "A 10 mW fully integrated 2-to-13 V-input buck-boost SC converter with 81.5% peak efficiency," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2016, pp. 224–225.

[34] W. Jung, D. Sylvester, and D. Blaauw, "A rational-conversion-ratio switched-capacitor DC-DC converter using negative-output feedback," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, pp. 218–219.

[35] W.-H. Ki, Y. Lu, F. Su, and C.-Y. Tsui, "Design and analysis of on-chip charge pumps for micro-power energy harvesting applications," in *Proc. IEEE/IFIP Int. Conf. VLSI Syst.-Chip*, Oct. 2011, pp. 374–379.

[36] T. Tanzawa, "On two-phase switched-capacitor multipliers with minimum circuit area," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 10, pp. 2602–2608, Oct. 2010.

[37] Y. Beck and S. Singer, "Capacitive transposed series-parallel topology with fine tuning capabilities," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 1, pp. 51–61, Jan. 2011.

[38] M. D. Seeman, "A design methodology for switched-capacitor DC-DC converters," Ph.D. dissertation, Dept. EECS, Univ. California, Berkeley, CA, USA, Tech. Rep. UCB/EECS-2009-78, May 2009.

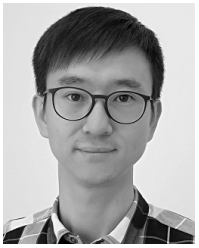
[39] Y. Jiang, M.-K. Law, P.-I. Mak, and R. P. Martins, "A 0.22-to-2.4 V-input fine-grained fully integrated rational buck-boost SC DC-DC converter using algorithmic voltage-feed-in (AVFI) topology achieving 84.1% peak efficiency at 13.2 mW/mm^2," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 422–423.

[40] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. JSSC-11, no. 3, pp. 374–378, Jun. 1976.

[41] H. Lee and P. K. T. Mok, "Switching noise and shoot-through current reduction techniques for switched-capacitor voltage doubler," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1136–1146, May 2005.

[42] F. Su, W. H. Ki, and C. Y. Tsui, "Regulated switched-capacitor doubler with interleaving control for continuous output regulation," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1112–1120, Apr. 2009.

[43] N. Lindert, T. Sugii, S. Tang, and C. Hu, "Dynamic threshold pass-transistor logic for improved delay at lower power supply voltages," *IEEE J. Solid-State Circuits*, vol. 34, no. 1, pp. 85–89, Jan. 1999.



Yang Jiang (S'13) received the B.Sc. and M.Sc. degrees in electrical and electronics engineering from the University of Macau, Macau, China, in 2009 and 2012, respectively, where he is currently pursuing the Ph.D. degree in electrical and computer engineering with the Electrical and Computer Engineering Department, Faculty of Science and Technology, and the State Key Laboratory of Analog and Mixed-Signal VLSI.

His current research interests include fully integrated dc power converters in bulk CMOS, especially on the design and analysis of switched-capacitor converter topologies with innovative techniques.

Man-Kay Law (M'11–SM'16) received the B.Sc. degree in computer engineering and the Ph.D. degree in electronic and computer engineering from the Hong Kong University of Science and Technology (HKUST), Hong Kong, in 2006 and 2011, respectively.

In 2011, he joined HKUST as a Visiting Assistant Professor. He was with the Zhejiang Advanced Manufacturing Institute, HKUST, where he developed an ultra-low-power fully integrated CMOS temperature sensing passive ultra-high frequency (UHF) radio frequency identification (RFID) tag together. He is currently an Associate Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, Faculty of Science and Technology, University of Macau, Macau, China. He has authored and co-authored over 80 technical journals and conference papers. He holds six U.S. patents. His current research interests include the development of ultra-low-power sensing circuits and integrated energy harvesting techniques for wireless and biomedical applications.

Dr. Law is a member of the Technical Program Committee of Asia Symposium on Quality Electronic Design, the IEEE International Symposium on Circuits and Systems (ISCAS), Biomedical Circuits and Systems Conference (BioCAS), International Symposium on Integrated Circuits (ISIC), a ITPC Member of the IEEE International Solid-State Circuits Conference (ISSCC), and the University Design Contest Co-Chair of Asia and South Pacific Design Automation Conference (ASPDAC). He was a co-recipient of the ASQED Best Paper Award in 2013, the A-SSCC Distinguished Design Award in 2015, and the ASP-DAC Best Design Award in 2016. He was a recipient of the Macao Science and Technology Invention Award (Second Class) by the Macau Government—FDCT in 2014 and 2018. He serves as a Technical Committee Member of the IEEE CAS Committees on Sensory Systems and the IEEE CAS Committee on Biomedical Circuits and Systems.

Pui-In Mak (S'00–M'08–SM'11) received the Ph.D. degree from the University of Macau (UM), Macau, China, in 2006.

He is currently a Full Professor with the Department of Electronic and Computer Engineering, Faculty of Science and Technology, UM, where he is also an Associate Director (Research) with the State Key Laboratory of Analog and Mixed-Signal VLSI. His current research interests include analog and radio frequency circuits and systems for wireless and multidisciplinary innovations.

Dr. Mak was the TPC Vice Co-Chair of ASP-DAC in 2016, a TPC Member of A-SSCC from 2013 to 2016, the ESSCIRC from 2016 to 2017, ISSCC since2016, and a member of Board-of-Governors of the IEEE Circuits and Systems Society from 2009 to 2011. He has been the Chair of the Distinguished Lecturer Program of IEEE Circuits and Systems Society since 2018. He was a co-recipient of the DAC/ISSCC Student Paper Award in 2005, the CASS Outstanding Young Author Award in 2010, the National Scientific and Technological Progress Award in 2011, the Best Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 2012 to 2013, the A-SSCC Distinguished Design Award in 2015, the ISSCC Silkroad Award in 2016, and the Honorary Title of Value for Scientific Merits by the Macau Government in 2005. He was an Editorial Board Member of the IEEE Press from 2014 to 2016. He was the Senior Editor of the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS from 2014 to 2015, an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS since 2018, IEEE SOLID-STATE CIRCUITS LETTERS since 2017, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I from 2010 to 2011 and from 2014 to 2015, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 2010 to 2013. He was a Distinguished Lecturer of the IEEE Circuits and Systems Society from 2014 to 2015 and the IEEE Solid-State Circuits Society from 2017 to 2018. He has been inducted as an Overseas Expert of the Chinese Academy of Sciences since 2018.

Rui P. Martins (M'88–SM'99–F'08) was born in 1957. He received the bachelor's, master's, Ph.D., and the Habilitation degrees for Full Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), University of Lisbon, Lisbon, Portugal, in 1980, 1985, 1992 and 2001, respectively.

Since 1980, he has been with the Department of Electrical and Computer Engineering, IST. Since 1992, he has been on leave from IST. He is currently with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macau, China, where he has been a Chair Professor since 2013. From 1994 to 1997, he was the Dean of the Faculty of the FST. Since 1997, he has been a Vice-Rector with the University of Macau. Since 2008, after the reform of the UM Charter, he has been nominated after open international recruitment, and reappointed (in 2013), as a Vice-Rector (Research). He was a Co-Founder of Chipidea Microelectronics (now Synopsys Macau), in 2011/2012. As the Founding Director, he created in 2003 the Analog and Mixed-Signal VLSI Research Laboratory of UM, which is elevated in 2011 to the State Key Laboratory of China (the 1st in Engineering in Macao). Within the scope of his teaching and research activities, he has taught 21 bachelor and master courses and, in UM, has supervised (or co-supervised) 45 theses, Ph.D. (24) and Masters (21). He has co-authored 7 books and 11 book chapters, 442 papers, in scientific journals (141) and in conference proceedings (301), and other 64 academic works, in a total of 554 publications. He holds 28 U.S. patents and 22 Taiwan patents.

Dr. Martins was a Nominations Committee Member of the IEEE Circuits and Systems Society (CASS) in 2016 and 2017 and a member of the IEEE CASS Fellow Evaluation Committee in 2013, 2014, and 2019. He was a Founding Chairman of both the IEEE Macau Section from 2003 to 2005 and the IEEE Macau Joint-Chapter on CAS/Communications from 2005 to 2008 (2009 World Chapter of the Year of IEEE CASS). He was the General Chair of the 2008 IEEE Asia–Pacific Conference on CAS—APCCAS'2008 and a Vice President of Region 10 (Asia, Australia, and the Pacific) of the IEEE CASS from 2009 to 2011. He was a Vice President (World) of the Regional Activities and a member of the IEEE CASS from 2012 to 2013. He has been a member of the IEEE CASS Fellow Evaluation Committee (2013, 2014, and 2019), and was the CAS Society Representative in the Nominating Committee, for the election in 2014, of Division I (CASS/EDS/SSCS)—Director of the IEEE. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference—ASP-DAC'2016. He was the Chair of the IEEE CASS Fellow Evaluation Committee (Class 2018). In the representation of UM was one of the Vice Presidents from 2005 to 2014 and the President from 2014 to 2017 of the Association of Portuguese Speaking Universities. In 2010 was elected, unanimously, as a Corresponding Member of the Portuguese Academy of Sciences in Lisbon, is the only Portuguese Academician living in Asia. He was a recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, the Honorary Title of Value from Macao successive approximation register (SAR) Government (Chinese Administration) in 2001, the IEEE Council on Electronic Design Automation Outstanding Service Award in 2016, and nominated the Best Associate Editor of TRANSACTIONS ON CAS II from 2012 to 2013. He served as an Associate Editor for the IEEE TCAS II: EXPRESS -BRIEFS from 2010 to 2013.