Letters

Subtraction-Mode Switched-Capacitor Converters With Parasitic Loss Reduction

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***Abstract*—In this letter, subtraction-mode switched-capacitor (SC) converters are proposed and analyzed. When compared to a conventional summation-mode SC converter, some of the flying capacitors of the subtraction-mode SC converters have reduced voltage swings, and hence the switching loss of the corresponding positive- and negative-plate parasitic capacitors is reduced, and efficiency is enhanced. The proposed subtraction-mode topologies use the same number of flying capacitors and switches as the summation-mode topologies, and they are reconfigured without using any auxiliary circuits, so there are no tradeoffs in terms of power density, cost, voltage conversion ratio (VCR), or equivalent output resistance. A test chip with VCRs of 1/3×, 2/3×, 3/4×, and 4/5× was fabricated in a 65-nm CMOS process. Efficiency improvement of more than 10% was achieved when compared to summation-mode designs.**

I. Introduction

FULLY integrated switched-capacitor (SC) converters are gaining demands in emerging applications such as low-power Internet-of-Things and system-on-chips. For low-power applications, capacitors are readily integrated on-chip, such that system form factor and cost are reduced. For fully integrated SC converters, power density, and efficiency are the important considerations, because they have direct impact on the standby time and the silicon area. A standard CMOS process has low on-chip capacitance density, and very high switching frequency (tens to hundreds of MHz) is used to reduce the output impedance and increase the power density, and results in high switching and parasitic loss, and degrades efficiency significantly.

Metal-oxide-semiconductor (MOS) capacitors are usually used in fully integrated SC converters, as they have the highest capacitance density among all on-chip capacitors, but they also have the largest parasitic capacitors. Fig. 1 shows two commonly used MOS capacitors: the NCAP and the PMOS capacitors. For the NCAP, the top-plate is the gate and the bottom-plate is the source/drain, and the main capacitor is C_g. The junction from P-substrate to N-well should be reverse-biased, forming the parasitic capacitor C_W across the junction J_W. P-substrate is connected to ground, and C_W will be charged and discharged as C_g switches and introduces parasitic loss. Similarly, for the PMOS capacitor, there are parasitic capacitors C_P and C_W across the diodes from drain/source to the N-well and the N-well to the P-substrate. These parasitic capacitors (C_P and C_W) are around 3%–5% of the gate capacitance. Junction capacitors are determined by doping concentrations of P-substrate and N-well, and stay relatively constant across different technology nodes. Hence, parasitic loss is quite significant as the operating frequency increases.

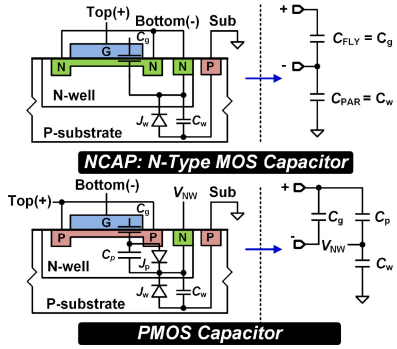

Fig. 1. Top- and bottom-plate parasitic capacitors of on-chip MOS capacitors.

Special techniques in achieving high capacitance density were reported, such as deep-trench capacitors [1], ferroelectric capacitors [2], and high-density MIM capacitors, but additional and costly processing steps are needed. An alternative method to reduce parasitic loss could be clever circuit design.

In CMOS process, the parasitic capacitance is voltage dependent on the body bias voltage. In [3] and [4], the N-wells of the MOS capacitors are left floating with a high impedance to ground or supply voltage, and the two parasitic capacitors are connected in series with respect to the substrate. If the N-wells are reverse-biased, then increasing the bias voltage reduces the

Manuscript received July 6, 2019; accepted August 3, 2019. Date of publication August 5, 2019; date of current version November 12, 2019. This work was supported by the Research Grants Council of the Theme-Based Research Scheme of Hong Kong under Project T23-612/12-R. *(Corresponding author: Junmin Jiang.)*

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Digital Object Identifier 10.1109/TPEL.2019.2933623

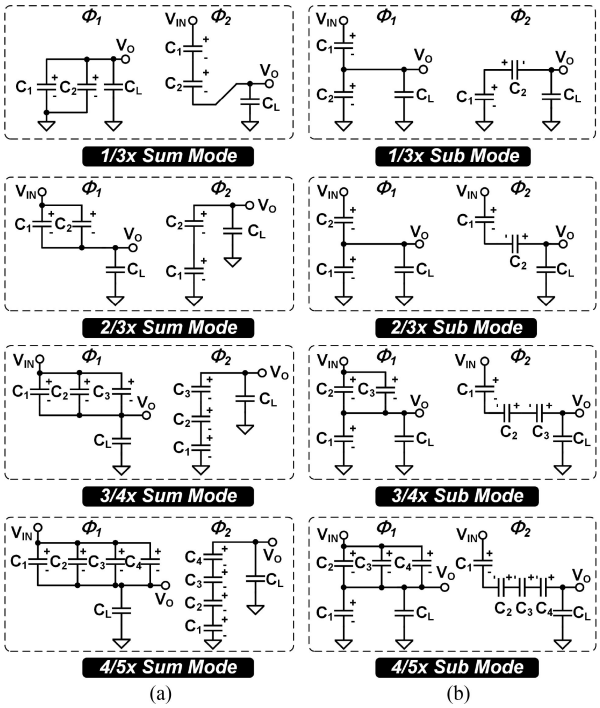

Fig. 2. Operating principle of (a) summation modes and (b) subtraction modes.

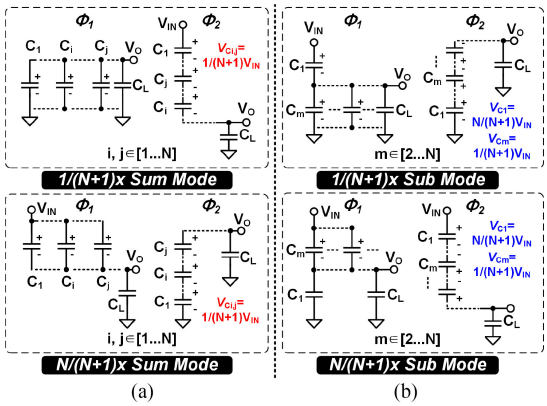

Fig. 3. Operating principle of general (a) $1/(N+1)\times$ and (b) $N/(N+1)\times$ SC converters.

junction capacitance, and the high bias voltage can be generated from an on-chip doubler [5] or an external voltage supply [6]. All the above methods require auxiliary power supplies and extra circuitry, which introduce extra cost. Besides, when the voltage conversion ratio (VCR) is small, the flying capacitors have larger voltage swings, and so do the corresponding parasitic capacitors, thus still incurring larger parasitic loss.

In this letter, we propose subtraction-mode SC converters that use the same number of flying capacitors and switches to achieve the same VCRs and output resistances, with flying capacitors having smaller voltage swings that result in lower parasitic loss. A test chip with both summation mode and subtraction mode in four commonly used VCRs: $1/3\times$, $2/3\times$, $3/4\times$, and $4/5\times$ was fabricated, for comparison.

II. Proposed Subtraction-Mode SC Converters

A. Summation-Mode Series-Parallel Topologies

Series-parallel topologies are the most commonly used topologies in state-of-the-art step-down SC converters. Fig. 2(a) shows the steady-state operations of SC converters with four typical VCRs ($1/3\times$, $2/3\times$, $3/4\times$, and $4/5\times$). Take the $1/3\times$ SC converter as an example, and consider the load current is negligible. In Φ_2 (the series phase), two flying capacitors C_1 and C_2 and the loading capacitor C_L are connected in series and charged up by the supply voltage $V_{\rm IN}$, and we have

$$\Phi_2 : V_{\rm IN} - V_O = V_{C2} + V_{C1}. \tag{1}$$

In Φ_1 (the parallel phase), C_1, C_2, and C_L are connected in parallel and all are discharged by load current, and

$$\Phi_1 : V_{C2} = V_{C1} = V_O. \tag{2}$$

Solving (1) and (2) gives $V_O = V_{C1} = V_{C2} = 1/3\,V_{\rm IN}$.

The above operations extend to similar $1/(N+1)\times$ and $N/(N+1)\times$ converters (N is flying capacitor numbers), as shown in Fig. 3(a). Note that in the parallel phase (Φ_1), all N flying capacitors are connected in parallel so they have same dc voltage $1/(N+1)\times {\rm V_{IN}}$. Then, in the series phase (Φ_2), all N flying capacitors $C_i (i = 1 \ldots N)$ are stacked in series with the positive-plate of C_i connected to the negative-plate of C_j, such that the voltage across all C_i in series is the "sum" of all capacitor voltages, and this is the reason of the name "summation mode." Clearly, for C_1, the voltage swing of the positive-plate and negative-plate is $N/(N+1)\times V_{\rm IN}$, and subsequent C_i has lower voltage swings. Hence, the parasitic capacitors of C_1 contribute the most to the parasitic loss.

B. Subtraction-Mode Topologies

Next, we propose an alternative method to generate step-down VCRs ($1/3\times$, $2/3\times$, $3/4\times$, and $4/5\times$) as shown in Fig. 2(b). Again, take the $1/3\times$ SC converter as an example. In Φ_1, C_1 is connected in series to the parallel-connected C_2 and C_L, and

$$\Phi_1 : V_{\rm IN} = V_{C2} + V_{C1} = V_{C1} + V_O. \tag{3}$$

In Φ_2, the negative-plate of C_1 is connected to ground, and the positive-plate is connected to C_2 (with a reversed polarity) and C_L in series, and

$$\Phi_2 : V_{C1} = V_{C2} + V_O \Rightarrow V_O = V_{C1} - V_{C2}. \tag{4}$$

Solving (3) and (4) gives $V_O = 1/3\,V_{\rm IN}$. Note that in the series phase (Φ_2), when C_1 and C_2 are viewed as connected in series, plates of the same polarity are connected together, such that the voltage across the two capacitors is the "difference" of their capacitor voltages, and hence the name of "subtraction mode." Fig. 2(b) shows the subtraction-mode converters with VCRs of $2/3\times$, $3/4\times$, and $4/5\times$, and their output voltages are

$$V_{O,2/3\times} = {\rm V_{IN}} - (V_{C2} - {\rm V_{C1}}) = 2/3 V_{\rm IN}. \tag{5}$$

$$V_{O,3/4\times} = {\rm V_{IN}} - (V_{C3} - {\rm V_{C2}} - {\rm V_{C1}}) = 3/4 V_{\rm IN}. \tag{6}$$

$$V_{O,4/5\times} = {\rm V_{IN}} - (V_{C4} - V_{C3} - V_{C2} - {\rm V_{C1}}) = 4/5 V_{\rm IN}. \tag{7}$$

TABLE I
COMPARISON OF VOLTAGE SWINGS OF EACH FLYING CAPACITOR

VCRs	Node	Summation Mode			Subtraction Mode		
		Φ_1	Φ_2	ΔV	Φ_1	Φ_2	ΔV
1/3×	C_1+	**1/3V_{IN}**	**V_{IN}**	**2/3V_{IN}**	**V_{IN}**	**2/3V_{IN}**	**1/3V_{IN}**
	C_1-	**0**	**2/3V_{IN}**	**2/3V_{IN}**	**1/3V_{IN}**	**0**	**1/3V_{IN}**
	C_2+	1/3V_{IN}	2/3V_{IN}	1/3V_{IN}	1/3V_{IN}	2/3V_{IN}	1/3V_{IN}
	C_2-	0	1/3V_{IN}	1/3V_{IN}	**0**	1/3V_{IN}	1/3V_{IN}
2/3×	C_1+	**V_{IN}**	**1/3V_{IN}**	**2/3V_{IN}**	**2/3V_{IN}**	**V_{IN}**	**1/3V_{IN}**
	C_1-	**2/3V_{IN}**	**0**	**2/3V_{IN}**	**0**	**1/3V_{IN}**	**1/3V_{IN}**
	C_2+	V_{IN}	2/3V_{IN}	1/3V_{IN}	V_{IN}	2/3V_{IN}	1/3V_{IN}
	C_2-	2/3V_{IN}	1/3V_{IN}	1/3V_{IN}	2/3V_{IN}	1/3V_{IN}	1/3V_{IN}
3/4×	C_1+	**V_{IN}**	**1/4V_{IN}**	**3/4V_{IN}**	**3/4V_{IN}**	**V_{IN}**	**1/4V_{IN}**
	C_1-	**3/4V_{IN}**	**0**	**3/4V_{IN}**	**0**	**1/4V_{IN}**	**1/4V_{IN}**
	C_2+	V_{IN}	1/2V_{IN}	1/2V_{IN}	V_{IN}	1/2V_{IN}	1/2V_{IN}
	C_2-	3/4V_{IN}	1/4V_{IN}	1/2V_{IN}	3/4V_{IN}	1/4V_{IN}	1/2V_{IN}
	C_3+	V_{IN}	3/4V_{IN}	1/4V_{IN}	V_{IN}	3/4V_{IN}	1/4V_{IN}
	C_3-	3/4V_{IN}	1/2V_{IN}	1/4V_{IN}	3/4V_{IN}	1/2V_{IN}	1/4V_{IN}
4/5×	C_1+	**V_{IN}**	**1/5V_{IN}**	**4/5V_{IN}**	**4/5V_{IN}**	**V_{IN}**	**1/5V_{IN}**
	C_1-	**4/5V_{IN}**	**0**	**4/5V_{IN}**	**0**	**1/5V_{IN}**	**1/5V_{IN}**
	C_2+	V_{IN}	2/5V_{IN}	3/5V_{IN}	V_{IN}	2/5V_{IN}	3/5V_{IN}
	C_2-	4/5V_{IN}	1/5V_{IN}	3/5V_{IN}	4/5V_{IN}	1/5V_{IN}	3/5V_{IN}
	C_3+	V_{IN}	3/5V_{IN}	2/5V_{IN}	V_{IN}	3/5V_{IN}	2/5V_{IN}
	C_3-	4/5V_{IN}	2/5V_{IN}	2/5V_{IN}	4/5V_{IN}	2/5V_{IN}	2/5V_{IN}
	C_4+	V_{IN}	4/5V_{IN}	1/5V_{IN}	V_{IN}	4/5V_{IN}	1/5V_{IN}
	C_4-	4/5V_{IN}	3/5V_{IN}	1/5V_{IN}	4/5V_{IN}	3/5V_{IN}	1/5V_{IN}

With no loss of generality, the flying capacitor that has the largest capacitor voltage, which is also connected to $V_{\rm IN}$ in one of the phases, is labeled as C_1 [see Fig. 2(b)].

To summarize, subtraction-mode SC converters with VCR $= N/(N+1)$ or $1/(N+1)$ can be generated using N flying capacitors, as shown in Fig. 3(b). In one phase, C_1 is charged to $V_{C1} = N/(N+1) \times V_{\rm IN}$, while the other flying capacitors C_M (M $\neq$ 1) have $V_{\rm CM} = 1/(N+1) \times V_{\rm IN}$. In another phase, if the negative-plate of C_1 is grounded, we have

$$V_O = V_{C1} - \sum_{M\neq 1} V_{\rm CM} = \frac{1}{N+1} V_{\rm IN}. \tag{8}$$

And if positive-plate of C_1 is connected to $V_{\rm IN}$, we have

$$V_O = V_{\rm IN} - \left(V_{C1} - \sum_{M\neq 1} V_{\rm CM} \right) = \frac{N}{N+1} V_{\rm IN}. \tag{9}$$

For a subtraction-mode SC converter, C_1 has a larger V_{C1}, and the voltage swings of its positive- and negative-plates (V_{C1+} and V_{C1-}, respectively) are thus lower. In fact, $\boldsymbol{\Delta} V_{C1+}$ and $\boldsymbol{\Delta} V_{C1-}$ are only 1/N of those of the summation mode counterparts. Table I summarizes the voltage swings of the positive- and negative-plates of the flying capacitors of the converters in Fig. 2. Recall that the parasitic capacitors of C_1 contribute the most to the parasitic loss, and now they have much reduced voltage swings, resulting in significant reduction of parasitic loss and improvement in efficiency. However, it should not be higher than the MOS's breakdown voltage. The voltage swings of the other flying capacitors remain the same in the two modes.

For two modes of SC converters, since the number of capacitors and switches, and the charges through each capacitors and switches are the same, steady-state performance such as the equivalent output resistance remains the same. In summary, subtraction-mode SC converters have lower parasitic loss, and no performance tradeoff in terms of power density.

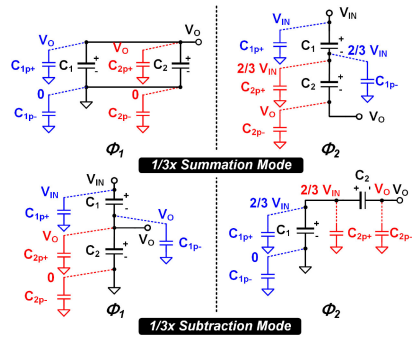

Fig. 4. Parasitic capacitors on top- and bottom-plate of 1/3× mode.

III. ANALYSIS OF PARASITIC LOSS

We then turn to the analysis of reduction in parasitic loss. We assume that the voltages of the flying capacitors are not affected by the charge introduced by the parasitic capacitors, as they are much smaller (usually below 5%) than the flying capacitors. No-load condition is also assumed such that the capacitor voltages do not change from phase to phase.

Let us consider the 1/3× SC converter as shown in Fig. 4. The positive- and negative-plate parasitic capacitors are C_{1p+}, C_{1p-}, C_{2p+}, and C_{2p-}, and their voltage swings in both phases are indicated. For the summation-mode converter, when Φ_1 changes to Φ_2, C_{1p+} is charged from V_O to $V_{\rm IN}$ with a charge Q_{1P+}. The energy sourced from $V_{\rm IN}$ is

$$E_{1P+,\rm CH} = V_{\rm IN} Q_{1P+} = V_{\rm IN} \left(V_{\rm IN} - V_O\right) C_{1P+} = \frac{2}{3} V_{\rm IN}^2 C_{1P+}. \tag{10}$$

When Φ_2 changes to Φ_1, C_{1p+} is discharged from $V_{\rm IN}$ to V_O, and the energy that is returned to V_O is

$$E_{1P+,\rm DIS} = V_{\rm O} Q_{1P+} = V_{\rm O} \left(V_{\rm IN} - V_O\right) C_{1P+} = \frac{2}{9} V_{\rm IN}^2 C_{1P+}. \tag{11}$$

The energy loss due to C_{1P+} is the difference of (10) and (11), and is given by

$$E_{1P+,\rm LOSS} = E_{1P+,\rm CH} - E_{1P+,\rm DIS} = \frac{4}{9} V_{\rm IN}^2 C_{1P+}. \tag{12}$$

For C_{1p-}, it is charged from 0 to 2/3 $V_{\rm IN}$ in Φ_2

$$E_{1P-,\rm CH} = \left(V_{\rm IN} - V_O\right) \frac{2}{3} V_{\rm IN} C_{1P-} = \frac{4}{9} V_{\rm IN}^2 C_{1P-}. \tag{13}$$

In Φ_1, all the charge is dumped back to ground by C_{1p-}, and hence the loss is given by

$$E_{1P-,\rm LOSS} = E_{1P-,\rm CH} = \frac{4}{9} V_{\rm IN}^2 C_{1P-}. \tag{14}$$

In general, consider the parasitic capacitor C_P that is charged and discharged between two voltages V_L to V_H. In the charging phase, the energy sourced from the system is

$$E_{P,\rm CH} = V_{\rm H} \left(V_H - V_L\right) C_P. \tag{15}$$

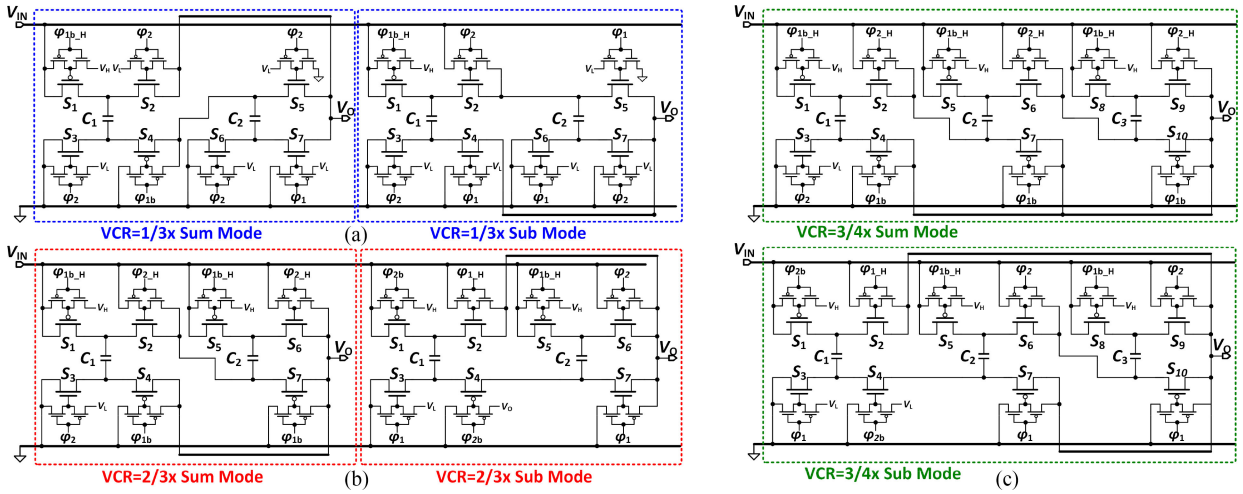

Fig. 5. Transistor implementation of both summation and subtraction modes with VCR of (a) 1/3×, (b) 2/3×, and (c) 3/4×.

TABLE II
ENERGY COSTED BY PARASITIC CAPACITORS

VCRs	Summation Mode	Subtraction Mode	Δ%
1/3×	$(5/9)V_{IN}^2(C_{p+}+C_{p-})$	$(2/9)V_{IN}^2(C_{p+}+C_{p-})$	60%
2/3×	$(5/9)V_{IN}^2(C_{p+}+C_{p-})$	$(2/9)V_{IN}^2(C_{p+}+C_{p-})$	60%
3/4×	$(7/8)V_{IN}^2(C_{p+}+C_{p-})$	$(3/8)V_{IN}^2(C_{p+}+C_{p-})$	57.14%
4/5×	$(6/5)V_{IN}^2(C_{p+}+C_{p-})$	$(3/5)V_{IN}^2(C_{p+}+C_{p-})$	50%

In the discharging phase, the energy returned to the system is

$$E_{P,\,\mathrm{DIS}} = V_L\,(V_H - V_L)\,C_P. \tag{16}$$

Hence, the energy of parasitic loss is

$$E_{P,\mathrm{LOSS}} = E_{P,\mathrm{CH}} - E_{P,\mathrm{DIS}} = (V_H - V_L)^2 C_P = \Delta V^2 C_P. \tag{17}$$

The same computation can be applied to the subtraction-mode converters.

By using (17), parasitic loss of all C_{ip+} and C_{ip-} $(i = 1 \ldots N)$ can be calculated using the voltage swings of the positive- and negative-plates of Table I, and the parasitic losses with different VCRs are compiled in Table II. Clearly subtraction-mode SC converters have reduced parasitic loss of 50%–60% when compared to summation-mode SC converters.

IV. TEST CHIP AND MEASUREMENT RESULTS

To verify the proposed concept and analysis, both summation-mode and subtraction-mode SC converters were designed and fabricated using the same circuit parameters for comparison. Fig. 5 shows the transistor-level schematics of three VCRs in the two modes. For 4/5×, the similar schematics are used. For each VCR, the SC converter of each mode uses the same number of flying capacitors and switches, and each has the same silicon area. The flying capacitors are implemented with stacked on-chip MIM, MOM, and MOS capacitors in a vertical hierarchy, and achieve a capacitance density of ∼10 fF/μm^2. A 2-phase clock passes through the nonoverlapping block, and the nonoverlapping phases are then level shifted to the proper voltage domains. Two voltage domains $V_L = 1.2$ V and

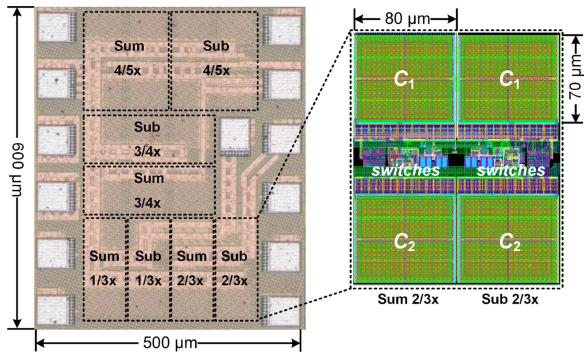

Fig. 6. Chip micrograph and the layout of 2/3× SC converters in two modes.

$V_H = V_{\mathrm{IN}} - 1.2$ V are generated by voltage regulators to tackle the breakdown issues. To have fair comparison, the switches in both the summation mode and the subtraction mode have almost the same turn-ON resistance. Test bits are used to individually enable each topology and select the respective output node for measuring the efficiency.

The test chip consisted of four VCRs was fabricated in a 65 nm CMOS process. It occupies a total area of 500 μm × 600 μm, as shown in Fig. 6. The two types of topologies occupied the same chip area. Fig. 7 shows the measured efficiencies of the step-down SC converters in both modes with VCRs of 1/3×, 2/3×, 3/4×, and 4/5×. The output voltages were kept the same to ensure that both types of converter delivered the same power. It is confirmed that for all VCRs, the proposed subtraction-mode converters achieved higher efficiency than the summation-mode converters across the entire loading range. For the converters with VCR $= 1/3 \times$ ($V_{\mathrm{IN}} = 2$ V, $V_O = 0.6$ V), switching and parasitic loss are most significant at light-load condition, the improvement in efficiency was as high as 20% [see in Fig. 7(a)]. For the converters working in different frequencies, the subtraction-mode converter achieved a 13% peak efficiency improvement when $f_{SW} = 60$ MHz, and an 11% peak efficiency improvement when $f_{SW} = 100$ MHz. Similar results were observed for 2/3×, 3/4×, and 4/5×, as shown in Fig. 7(b)–(d). Efficiency improvement is always larger for converters operating

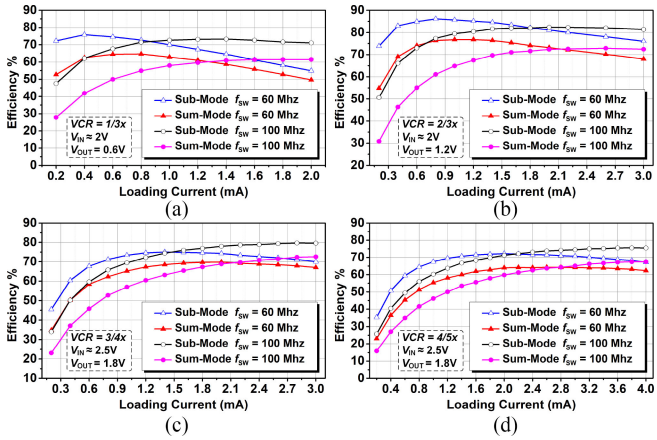

Fig. 7. Measured efficiency of summation- and subtraction-mode converters at 60 and 100 MHz.

at higher switching frequency, and is consistent with the analysis shown in Section III.

V. Conclusion

This letter proposed subtraction-mode SC converters that use the same number of flying capacitors and switches as the summation-mode converters, but have reduced positive- and negative-plate voltage swings. Measurement results verified that significant efficiency improvement was achieved, thanks to the reduced parasitic loss, and there are no tradeoffs in terms of power density, cost, VCR, or equivalent output resistance.

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