A 0.0056-mm^2 −249-dB-FoM All-Digital MDLL Using a Block-Sharing Offset-Free Frequency-Tracking Loop and Dual Multiplexed-Ring VCOs

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***Abstract*— This paper describes an ultra-compact all-digital multiplying delay-locked loop (MDLL) featuring a low-power block-sharing offset-free frequency-tracking loop (FTL) to calibrate the process–voltage–temperature variations of the voltage-controlled oscillator (VCO) frequency. Such FTL utilizes a digital-controlled delay line (DCDL)-based low-power time-interval comparator and an adjacent-edge selector, to precisely detect the static phase offset (SPO) caused by the VCO frequency drifting in the presence of reference injection. The block-sharing-based SPO detection aids nullifying the circuit-mismatch- and offset-induced deterministic error. Also, for the adjacent edge selector, block sharing between its control generation circuits and the coarse FTL further reduces the power consumption. The varactor-tuned dual multiplexed-ring VCOs (MRVCOs) serve to reduce jitter variation while extending the frequency tuning range. Fabricated in a 28-nm CMOS with a core area of 0.0056 mm^2, the proposed MDLL covers a tuning range from 1.55 to 3.35 GHz, and exhibits a root-mean-square (rms) jitter of 292 fs at 3-GHz output, under a 200-MHz reference clock. The power consumption is 1.45 mW at a 0.8-V supply, resulting in an FoM of −249 dB favorably comparable with the state of the art.**

***Index Terms*— Clock multiplier, digital-controlled delay line (DCDL), frequency-tracking loop (FTL), injection-locked phase-locked loop (IL-PLL), multiplying delay-locked loop (MDLL), phase noise, ring voltage-controlled oscillator (RVCO), root-mean-square (rms) jitter.**

Manuscript received April 25, 2018; revised July 9, 2018 and August 23, 2018; accepted September 3, 2018. Date of publication October 1, 2018; date of current version January 14, 2019. This work was supported in part by Macao Science and Technology Development Fund through SKL Fund, and in part by the University of Macau under Grant MYRG2017-00185-AMSV. This paper was approved by Guest Editor Wim Dehaene. *(Corresponding author: Jun Yin.)*

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Digital Object Identifier 10.1109/JSSC.2018.2870551

I. Introduction

THE ultra-scaled CMOS technologies has motivated the development of all-digital phase-locked loop (ADPLL) with low-jitter, small area, and power [1]. To facilitate the system-on-chip (SoC) integration, recent efforts on clock-generation circuits favor the ring voltage-controlled oscillator (RVCO) for its large frequency tuning range, tiny area, and freedom from magnetic pulling. Regrettably, the limited phase noise performance of the RVCO penalizes the overall jitter performance, if a typical type-II phase-locked loop (PLL) with a ∼10%-f_{REF} loop bandwidth (BW) is employed to suppress the RVCO phase noise, where f_{REF} is the reference frequency. Thus, clock multipliers based on the injection-locked VCOs [2]–[14] gained high attention recently, as their loop BW can be extended to 25% of f_{REF} by directly replacing the noisy VCO output edge (OUT) with a clean edge from the reference clock (REF). An enlarged loop BW reduces effectively the RVCO phase noise, so as the overall jitter performance.

Fig. 1(a) shows the basic architecture of a multiplying delay-locked loop (MDLL) [8]–[14]. It can be considered as a type of hard injection-locked VCO, where the output frequency f_{OUT} is aimed to lock to the targeted frequency $f_{LOCK} = N \times f_{REF}$. The 1st to $(N-1)$th output periods of the MDLL within one REF cycle will be equal to $T_0 = 1/f_{VCO}$, where f_{VCO} is the frequency of the open-loop RVCO. Meanwhile, the last period will be abruptly changed to $T_1 = T_{REF} - (N-1)T_0$ due to the edge replacement as illustrated in Fig. 1(b). If f_{VCO} deviates from f_{LOCK} due to the process–voltage–temperature (PVT) variations [4], [5], a static phase offset (SPO) occurs ($T_1 \neq T_0$), which would cause an REF spur at the MDLL output. For a large deviation between f_{VCO} and f_{LOCK}, the MDLL may lock to a wrong frequency, i.e., the average f_{OUT} no longer tracks f_{LOCK}. Thus, a frequency-tracking loop (FTL) is essential for an MDLL such that f_{VCO} can stay close to f_{LOCK} in the presence of PVT variations. In [10] and [11], a bang-bang phase detector (BBPD) is employed to extract the phase difference between REF and OUT. Yet, the offset of the BBPD and the delay mismatch between the BBPD and

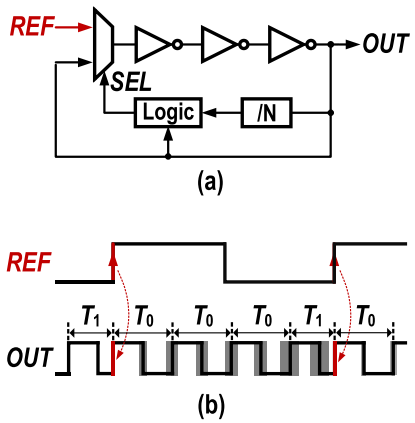


Fig. 1. (a) Block diagram and (b) timing diagram of a typical MDLL.

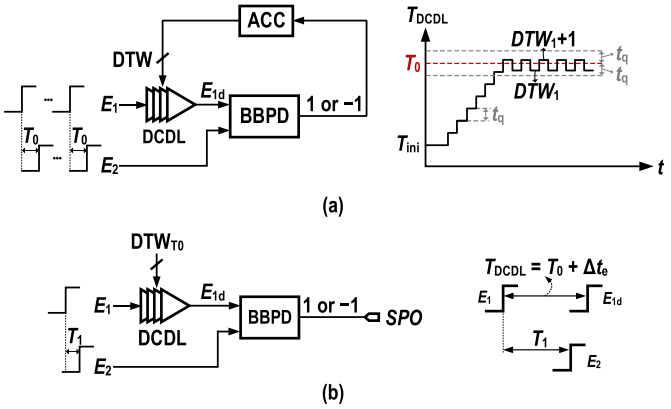


Fig. 2. DCDL-based SA time-length digitization and comparison scheme. (a) DCDL calibration step. (b) T_0/T_1 comparison step.

the multiplexer (MUX) paths limit the detection accuracy. The work from [12] resolves the SPO by calculating the period's error rate, but calls for power-hungry digital logics (3.5 mW) for the *in situ* time-domain mismatch-detection algorithm. In [13], T_0 and T_1 are quantized by a TDC and subtracted in the digital domain to obtain the SPO. Yet, the required high-resolution TDC is power hungry as well. In [14], the time lengths of T_0 and T_1 are converted to the voltage domain such that they can be compared by a single analog comparator to save the power consumption. Still, the analog circuits in the pulsewidth comparator and digital-to-analog converter (DAC) for offset calibration occupy a substantial amount of area (0.015 mm^2).

Aiming to extract accurately the timing error between T_0 and T_1 in the digital domain with low power consumption, the proposed MDLL [15] utilizes an adjacent edge selector and a time-interval comparator to extract, store, and compare T_0 and T_1, in order to nullify the effect induced by the circuit offset, while ensuring precise frequency tracking with low power. The circuit blocks for the coarse FTL are reused to generate the control signals for the adjacent edge selector, which further reduces the power consumption. Besides, we use dual multiplexed RVCOs (MRVCOs) with varactor tuning to maintain a constant root mean square (rms) jitter performance over the frequency tuning range. The die area becomes ultra-compact via block-sharing in the FTL, and a wideband frequency-tuning scheme that enables seamless switching among the three sub-division banks.

Section II presents the proposed low-power offset-free FTL. Section III discusses the MRVCOs design and the wideband frequency-tuning scheme that can enable a constant jitter performance over a wide frequency tuning range. Section IV analyzes the phase noise of the MDLL. Section V shows the experimental results, and finally we draw the conclusions in Section VI.

II. Proposed Low-Power Offset-Free FTL

A. DCDL-Based Time Storage and Comparison Scheme

Since the adjacent edges of OUT that carry the information of T_0 and T_1 do not appear simultaneously, we can store the time length of T_0 (T_1) first, and then compare it with T_1 (T_0). Using a high-resolution TDC to directly digitize T_0 and T_1 [13] is power inefficient since the TDC has to cover a large input range which will only be used during the frequency-locking process. After the MDLL is locked, the TDC output will be stable with a small variation.

To improve the power efficiency, we consider a digital-controlled delay line (DCDL)-based successive approximation (SA) scheme to digitize a certain time length [Fig. 2(a)]. Here, we use the DCDL with a delay time of T_{DCDL} to delay the early edge E_1 and the BBPD, and the feedback loop will automatically adjust the T_{DCDL} until the two edges $E_{1\mathrm{d}}$ and E_2 are close enough. Assuming the time intervals between the two input edges E_1 and E_2 is T_0, the settled DCDL control code DTW will jump between the two adjacent values D_1 and D_2, and the corresponding time error Δt_e between T_{DCDL} with T_0 will be smaller than one DCDL step t_q, as shown in Fig. 2(a). Either the control code DTW_1 or $\mathrm{DTW}_1 + 1$ can be stored as DTW_{T0} which sets T_{DCDL} close to T_0 with a maximum quantization error of t_q. The proposed SA scheme allows significant power savings by replacing the high-resolution TDC with a low-power DCDL and BBPD, but at the cost of a longer DCDL calibration time. To speed up the comparison of T_0 and T_1 once the DTW_{T0} has been found, we do not repeat the same procedure to find $\mathrm{DTW_{T1}}$ and compare it with $\mathrm{DTW_{T0}}$. Instead, we set the DCDL control code to $\mathrm{DTW_{T0}}$ and send the input edges E_1 and E_2 with a delay of T_1 to the time-interval comparator as exhibited in Fig. 2(b). As a result, T_0 and T_1 can be directly compared by the BBPD with one single comparison. Fig. 3 shows the complete block diagram of the time-interval comparator with the de-MUX implemented by logic gates to set the inactive output to zero. These will convey the BBPD output to the either feedback loop during the DCDL calibration step to find the $\mathrm{DTW_{T0}}$, or directly to the SPO during the T_0/T_1 comparison step.

Fig. 3 also presents the inputs E_1 and E_2 to the time-interval comparator generated by extracting the adjacent two rising edges from the OUT through $\mathrm{DFF_{1,2}}$. To produce E_1 and E_2 with a delay of T_0, we can choose CKR to control the reset RST of $\mathrm{DFF_{1,2}}$ (RST = CKR). By using the falling edge of OUT to retime REF, we can produce CKR which can guarantee enough time margin from the reset port to the clock

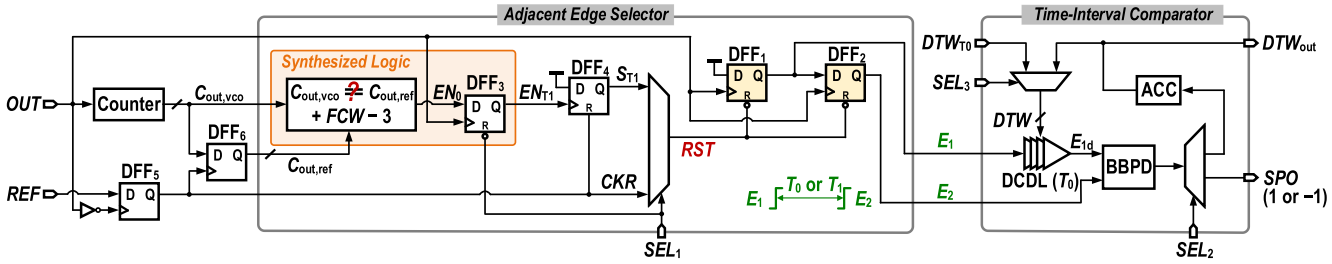


Fig. 3. Block diagram of the adjacent edge selector with the control signals and time-interval comparator.

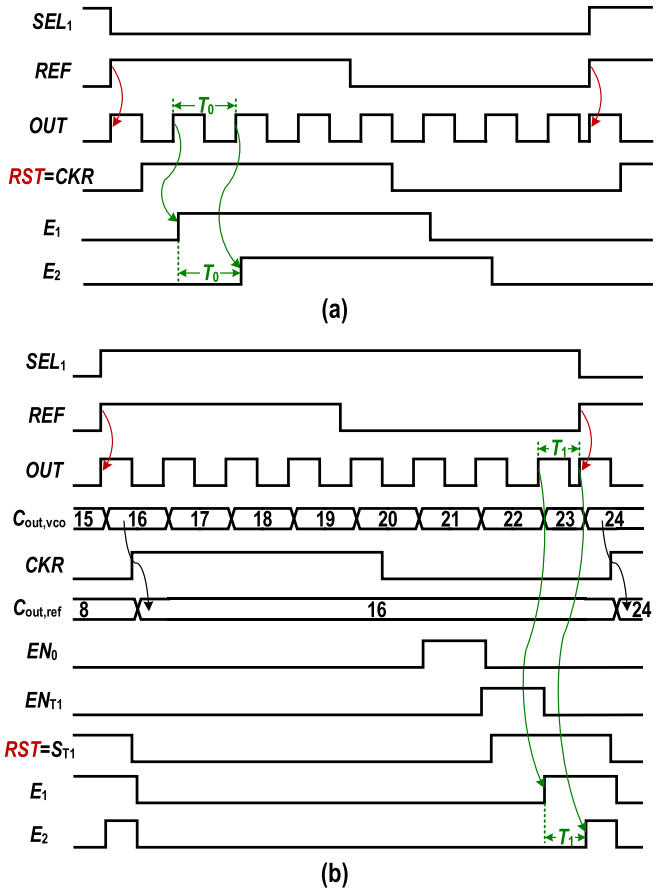


Fig. 4. Timing diagram of the adjacent edge selector to select E_1 and E_2 with a delay of (a) T_0 and (b) T_1 (FCW = 8).

port of DFFs to avoid metastability. Therefore, the two rising edges of OUT occurring right after the rising edge of REF can be properly selected [Fig. 4(a)]. To produce E_1 and E_2 with a delay of T_1, the (FCW − 1)th and FCWth rising edges of OUT occurring after the rising edge of REF must be precisely selected, which can be obtained with the aid of a counter that continuously computes the rising edges of OUT (Fig. 3). By comparing the counter output $C_{\text{out,vco}}$ with the ($C_{\text{out,ref}}$ + FCW − 3), the reset signal of $\text{DFF}_{1,2}$ (RST = S_{T1}) will be released right after the (FCW − 2)th rising edge of OUT, to ensure the correct selection of the (FCW − 1)th and FCWth rising edges of OUT [Fig. 4(b)]. To avoid metastability of $\text{DFF}_{1,2}$, the delay from the rising edge of OUT to the rising edge of RST must be shorter than one VCO cycle. Hence, we insert a DFF_3 clocked by OUT after the comparison logic to break the long path from OUT to RST (Fig. 3). Besides, the comparison logic and DFF_3 are synthesized separately from other digital logics operating at REF clock frequency to optimize the delay. We use the DFF_4 to extend the time duration of the RST signal staying at the high-voltage level since the DFF_3 output EN_{T1} can only stay at the high-voltage level for one VCO period. The reset signals of DFF_3 (active low) and DFF_4 (active high) controlled by SEL_1 and CKR are properly released several VCO periods before the rising edge of EN_0 and EN_{T1} [Fig. 4(b)]. According to the post-layout simulation, the delay times from the rising edge of OUT to the rising edge of EN_0 and to the rising edge of RST (RST = S_{T1}) are 198 and 114 ps, respectively, which ensures enough margin to avoid metastability in DFF_3 and $\text{DFF}_{1,2}$ even at $f_{\text{VCO}} = 3.2$ GHz. Since we utilize only the rising edges of $\text{DFF}_{1,2}$ to generate E_1 and E_2, the unbalanced rising and falling times of the DFF's output would not affect the SPO measurement. We connect the reset pins of $\text{DFF}_{5,6}$ (not shown in Fig. 3) to the global reset signal for the digital circuits, which will be released when the FTL starts to work.

The clock-to-output-delay mismatch between DFF_1 and DFF_2 (ΔT_{DFF}) and the offset of BBPD (ΔT_{BBPD}) may cause a deterministic comparison error. During the DCDL calibration step, the actual DCDL delay can be given by

$$T_{\text{DCDL}} = T_0 + \Delta t_e + \Delta T_{\text{DFF\_os}} + \Delta T_{\text{BBPD}}. \tag{1}$$

Since we reuse the same DFFs and BBPD during the T_0/T_1 comparison step, the net time difference detected by the time-interval comparator is

$$\begin{aligned} \Delta T_{\text{actual}} &= T_1 + \Delta T_{\text{DFF\_os}} + \Delta T_{\text{BBPD}} - T_{\text{DCDL}} \\ &= T_1 - T_0 - \Delta t_e. \end{aligned} \tag{2}$$

With the block sharing, we eliminate the effects of ΔT_{DFF}, ΔT_{BBPD}; thus, the accuracy of T_0/T_1 comparison is only limited by the quantization error Δt_e of the DCDL.

The quantization error from the DCDL and from the DAC and VCO will limit the *REF* spur performance. The REF spur of the MDLL can be estimated based on Fourier analysis [13]

$$\text{REF Spur} \approx 20 \log \left(\frac{|T_1 - T_0|}{T_{\text{OUT}}} \right) \tag{3}$$

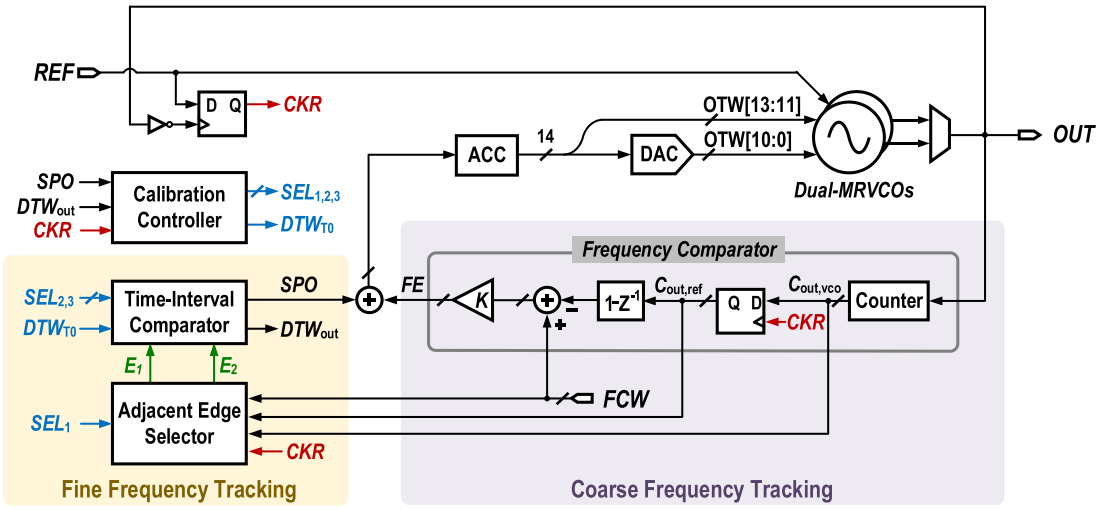


Fig. 5. Block diagram of the proposed all-digital MDLL.

where $T_{\rm OUT} = 1/f_{\rm OUT}$ and $f_{\rm OUT}$ is the desired output frequency. When the MDLL is properly locked, we have

$$({\rm FCW} - 1) \times T_0 + T_1 = {\rm FCW} \times T_{\rm OUT}. \tag{4}$$

According to (3) and (4), the REF spur becomes

$${\rm REF\ Spur} \approx 20 \log \left(\frac{f_{\rm DEV}}{f_{\rm REF}} \right) \tag{5}$$

where $f_{\rm DEV} = |f_{\rm OUT} - f_{\rm VCO}|$ is the frequency deviation between the actual VCO frequency and the desired output frequency. In the proposed MDLL, the FTL ensures $|T_1 - T_0| \leq t_q$ if the quantization error from the DAC and the VCO is negligibly small. The largest $f_{\rm DEV}$ occurs when $|T_1 - T_0| = t_q$. If we assume that $f_{\rm VCO} < f_{\rm OUT}$, i.e., $T_0 T_1 = t_q$, the VCO frequency can be obtained according to (4) and with $f_{\rm VCO} = 1/T_0 = {\rm FCW}/({\rm FCW} \times T_{\rm OUT} + t_q)$. Hence, the largest frequency deviation is $f_{\rm DEV} \approx f_{\rm OUT}^2 \times t_q/{\rm FCW}$. By considering the quantization error from the DAC and the VCO, the largest frequency deviation will further increase to $f_{\rm DEV} = f_{\rm OUT}^2 \times t_q/{\rm FCW} + K_{\rm DAC} K_{\rm VCO}$, where $K_{\rm DAC}$ and $K_{\rm VCO}$ are the DAC step and the VCO gain, respectively. Putting the $f_{\rm DEV}$ expression into (5), the worst case REF spur due to the quantization effect from DCDL and from DAC and VCO can be estimated as

$${\rm REF\ Spur} \approx 20 \log \left(f_{\rm OUT} \times t_q + \frac{K_{\rm DAC} K_{\rm VCO}}{f_{\rm REF}} \right). \tag{6}$$

In this paper, $t_q \approx 350$ fs and $K_{\rm DAC} K_{\rm VCO} \approx 210$ kHz results in a worst case spur level of −53.5 dBc. For small t_q and $K_{\rm DAC} K_{\rm VCO}$, the VCO phase noise will further contribute to the randomization of the REF spur.

B. Proposed MDLL Architecture

Fig. 5 exhibits the block diagram of the proposed MDLL that comprises mainly a count-based frequency comparator for coarse frequency tracking, an adjacent edge selector, and a time-interval comparator for fine frequency tracking. The power-hungry high-frequency counter and the REF retiming DFF are also reused to generate the input signals, i.e., $C_{\rm out,vco}$, $C_{\rm out,ref}$, and CKR (Fig. 3), to the adjacent edge selector, which reduces the power consumption. The calibration controller determines the digital control signals for the adjacent edge selector and time-interval comparator.

When the MDLL is enabled, the frequency comparator will be first started to bring the MRVCO frequency within the range of $({\rm FCW} - 1) \times f_{\rm REF} < f_{\rm VCO} < ({\rm FCW} + 1) \times f_{\rm REF}$. Then, the REF injection and fine frequency tracking will be activated. Fig. 6 illustrates the timing diagram of the fine frequency tracking. In the first phase of DCDL calibration, the delay of the DCDL in the time-interval comparator is continuously adjusted to T_0 every REF cycle according to the BBPD output. In the second phase of frequency tracking, the time-interval comparator will perform T_0/T_1 comparison, and the resulted SPO will be used to correct the VCO frequency. Since both T_0 and T_1 will change after the adjustment of the VCO frequency, the DCDL calibration and the T_0/T_1 comparison will be scheduled in an interleaved manner every REF cycle until the MRVCO frequency is locked ($T_0 = T_1$). After that, both the coarse and fine FTLs will keep operating in the background to continuously correct the MRVCO frequency error induced by the voltage and temperature variations.

III. Dual Multiplexed-Ring VCOs and the Wideband Frequency-Control Scheme

The proposed MDLL employs dual MRVCOs controlled by a DAC (Fig. 5) to extend the frequency tuning range. The varactor-tuning scheme helps keeping a constant rms jitter performance over the frequency tuning range as detailed next.

A. Varactor-Tuned Dual MRVCOs

The rms jitter of the MDLL can be obtained by integrating the output phase noise from offset frequencies f_1 and f_2

$$\sigma_{\rm rms} = \frac{\sqrt{2 \int_{f_1}^{f_2} \mathcal{L}_{\rm MDLL}(\Delta f) d(\Delta f)}}{2\pi f_{\rm LOCK}} \tag{7}$$

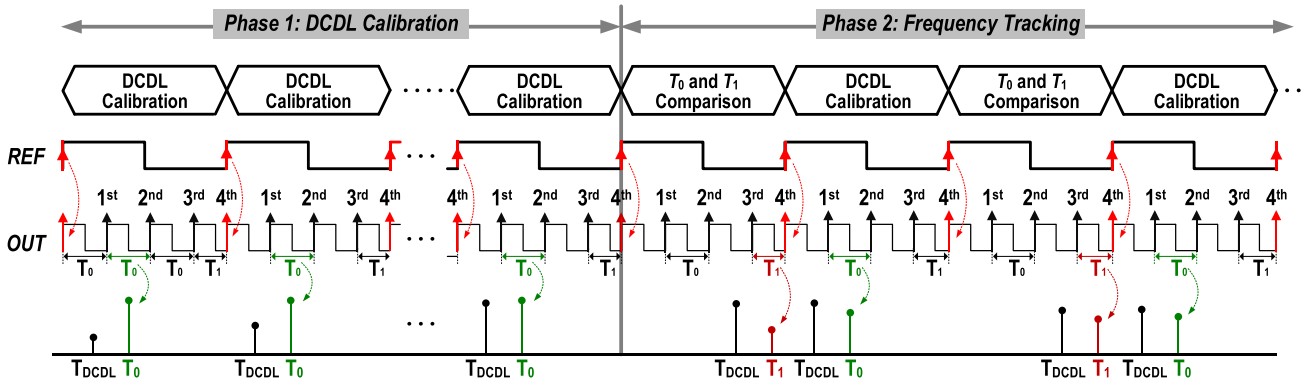


Fig. 6. Workflow of the fine FTL at FCW = 4.

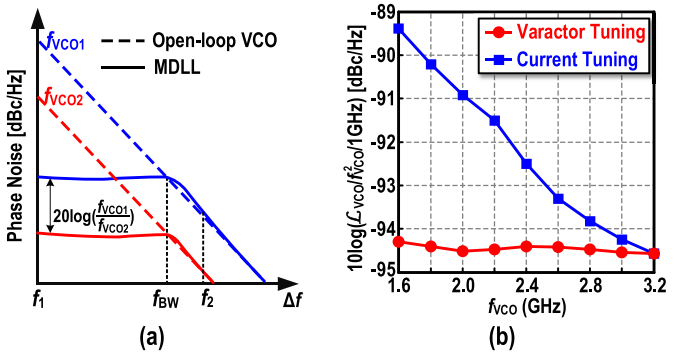


Fig. 7. (a) Phase noise scaling with the frequency to keep a constant rms jitter performance, and (b) comparison of the normalized RVCO phase noise between the varactor- and current-tuning schemes.

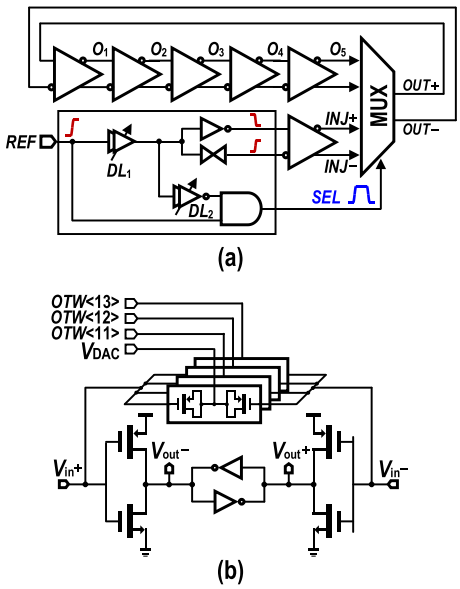


Fig. 8. Schematic of (a) MRVCO and (b) its delay cell.

where $\mathcal{L}_{\mathrm{MDLL}}(\Delta f)$ is the MDLL output phase noise at the offset frequency Δf. For an ideal MDLL ignoring the noises from the FTL and *REF*, $\mathcal{L}_{\mathrm{MDLL}}$ is only determined by the VCO phase noise $L_{\mathrm{VCO}}(\Delta f)$ and the BW f_{BW} caused by the REF injection. If, for simplicity, we only consider the $1/f^2$ noise of the VCO [Fig. 7(a)], the rms jitter of the MDLL when the VCO frequency is properly locked can be re-expressed as

$$\sigma_{\mathrm{rms}} = \frac{\sqrt{2(f_{\mathrm{BW}}-f_1)\mathcal{L}_{\mathrm{VCO}}(f_{\mathrm{BW}})+2\int_{f_{\mathrm{BW}}}^{f_2}\mathcal{L}_{\mathrm{VCO}}(\Delta f)d(\Delta f)}}{2\pi f_{\mathrm{VCO}}}. \tag{8}$$

Since f_{BW} is determined by f_{REF} and can be kept unchanged with the output frequency, the normalized phase noise $\mathcal{L}_{\mathrm{VCO}}(\Delta f)/f_{\mathrm{VCO}}^2$ must be kept constant in order to maintain a constant σ_{rms} when f_{VCO} changes. The thermal-noise-induced phase noise of an inverter-based RVCO can be obtained as [16]

$$\frac{\mathcal{L}_{\mathrm{VCO}}(\Delta f)}{f_{\mathrm{VCO}}^2} \approx \frac{8\Upsilon}{3\eta}\times\frac{kT}{I_{\mathrm{DC}}V_{\mathrm{ov}}}\times\frac{1}{\Delta f^2} \tag{9}$$

where I_{DC} is the current consumption of the RVCO, V_{ov} and γ are the overdrive voltage and the channel noise factor of MOS transistors, respectively, and η is the proportional constant. Assuming the power consumption dominated by the switching power such that $f_{\mathrm{VCO}} = (2I_{\mathrm{dc}})/(MC_{\mathrm{L}}V_{\mathrm{DD}})$, where M is the number of delay stages and C_{L} is the load capacitance of each delay stage, f_{VCO} can be changed by either tuning the current I_{DC} [2], [4]–[6], [8]–[11], [13], [14] or the load capacitor C_{L} [12]. According to (9) and the simulation results from Fig. 7(b), the current tuning method suffers from a degraded normalized phase noise at low frequency, while the capacitor tuning method can preserve the normalized phase noise constant.

The limited frequency tuning range of the capacitor tuning scheme can be compensated by using multiple RVCOs with little area penalty. In this paper, we utilize two five-stage varactor-tuned MRVCOs [Fig. 8(a)] to extend the frequency tuning range. The pseudodifferential inverter-based delay cells used in both MRVCOs have the same circuit topology which employs a 3-bit binary-weighted accumulated-MOS varactor bank for coarse frequency tuning and a small varactor controlled by the DAC for fine frequency tuning [Fig. 8(b)]. By choosing different transistors and varactor sizes for the delay cells, the two MRVCOs together can cover two frequency bands from 1.55 to 2.47 GHz and 2.35 to 3.35 GHz,

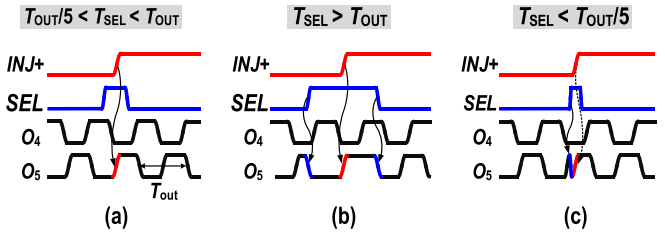


Fig. 9. Effect of the window length T_{SEL} on the MDLL output. (a) Correct window length of $T_{OUT}/5 < T_{SEL} < T_{OUT}$. (b) Oversized window length of $T_{SEL} > T_{OUT}$. (c) Undersized window length of $T_{SEL} < T_{OUT}/5$.

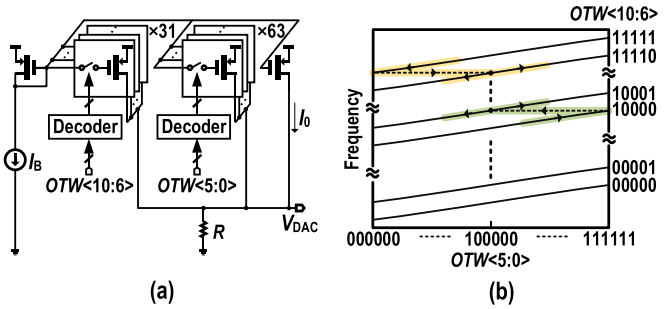


Fig. 10. (a) Schematic of the DAC and (b) illustration of seamless band switching frequency control between the medium and fine DAC banks.

with a 120-MHz overlap. They consume ∼1.45 mA over the frequency range of 1.55–3.35 GHz, and exhibit an open-loop phase noise of −85 dBc/Hz at 1 MHz offset and 3-GHz carrier frequency. Since the varactor-tuned MRVCO features a full swing output, a low-power inverter-based MUX (∼20 μW) can be used to select the desired output (Fig. 5). The un-used MRVCO is turned off to save power. The inverter-based ring RVCOs usually suffer from supply sensitivity which is ∼6500 MHz/V at a 3-GHz carrier in this paper. In practice, we need a low-dropout (LDO) regulator to stabilize its supply voltage [21].

The SEL signal in the MRVCO is generated directly through the REF [Fig. 8(a)]. The rising edge of REF is placed in the middle of the pulse SEL by properly adjusting the delay lines DL_1 and DL_2. The window length of SEL has to satisfy the condition: $T_{OUT}/N < T_{SEL} < T_{OUT}$, as illustrated in Fig. 9(a). It means that the upper limit is the condition not blocking the transition of the edges in the RVCO right before and after the REF injection [Fig. 9(b)]. We choose the lower limit to avoid the glitch caused by the competition between the RVCO edge generated by its former stage and the injected REF edge [Fig. 9(c)].

B. DAC-Based Wideband Frequency Tuning Using Seamless Band Switching Control

To attain a wide frequency tuning range while keeping a small frequency step is not trivial. In this design, each RVCO aims to cover a frequency range of ∼1 GHz. Even with the help of a 3-bit binary coarse-tuning varactor bank, a 10-bit DAC is required to cover a 240-MHz frequency range with a 240-kHz frequency step. To save the die size, we implemented the DAC with two thermometer-coded tuning banks which are controlled by OTW⟨10:6⟩ (medium bank) and OTW⟨5:0⟩ (fine bank), respectively [Fig. 10(a)]. To track the voltage and temperature variations after the frequency is locked, we use a seamless band switching control to keep the monotonic frequency change, even if OTW drifts at the boundary between the two tuning banks. To enable the seamless band switching logic, we design the whole frequency range of the fine bank to cover around twice of one frequency step of the medium bank. Consequently, the DAC in Fig. 10(a) has a 10-bit effective resolution. As Fig. 10(b) presents, when OTW⟨5:0⟩ is full of logic 1 and needs to be further increased, OTW⟨10:6⟩ will be raised by 1 and OTW⟨5:0⟩ will restart to change from the middle point, i.e., OTW⟨5:0⟩ = 6′ b100000 (instead of OTW⟨5:0⟩ = 6′ b000000), which can avoid the OTW to come back and forth across the boundary between the medium and fine banks. We also employed a similar band switching control at the boundary between the medium (OTW⟨10:6⟩) and the coarse (OTW⟨13:11⟩) banks.

IV. Analysis of Phase Noise

This section aims to develop a noise model for the proposed MDLL which helps analyzing the noise contribution from individual building block. Fig. 11 shows the generalized noise model where N is the multiplying ratio. We assume that the DCDL resolution is fine enough. For the reference injection part, we adopted the model from [5] and [17] by setting the phase realigning factor $\beta = 1$ for the MDLL

$$H_{UP} = N \times e^{-\frac{j\omega T_{REF}}{2}} \times \frac{\sin\left(\frac{\omega T_{REF}}{2}\right)}{\frac{\omega T_{REF}}{2}} \tag{10}$$

$$H_{RL1} = 1 - e^{-\frac{j\omega T_{REF}}{2}} \times \frac{\sin\left(\frac{\omega T_{REF}}{2}\right)}{\frac{\omega T_{REF}}{2}} \tag{11}$$

$$H_{RL2} = 1 - e^{-j\omega T_{REF}} \times e^{-\frac{j\omega T_{REF}}{2}} \times \frac{\sin\left(\frac{\omega T_{REF}}{2}\right)}{\frac{\omega T_{REF}}{2}}. \tag{12}$$

Here, H_{UP} represents the up-conversion of the reference noise to the output, and H_{RL1} and H_{RL2} represent the effect of the phase-realignment by the REF injection [5]. Since $\theta_{VCO,FR}$ represents the phase of the free-running VCO within the current RFE cycle, the phase information $\theta_{MDLL,NOI}$ of the MDLL at the time when the next REF edge comes (but does not inject yet) can be obtained by adding the $\theta_{VCO,FR}$ and the phase of the current REF edge. Thus, the difference between T_0 and T_1, i.e., θ_{SPO}, can be found by subtracting $\theta_{MDLL,NOI}$ from θ_{OUT}. Since we perform the T_0/T_1 comparison every two REF cycles in this design, θ_{SPO} is scaled down by $2N$ times when referred to the REF frequency.

Assuming DCDL step and $K_{DAC}K_{VCO}$ are small enough, implying that the random input noise of the BBPD dominates over the limit cycle, the BBPD can be modeled as a linear gain $K_{BBPD} = \sqrt{2}/(\sqrt{\pi} \times \sigma_{\Delta t})$ plus an additive quantization noise $S_{n,BBPD}$ [18], [19], where $\sigma_{\Delta t}$ is the standard deviation of the input time difference which can be well approximated

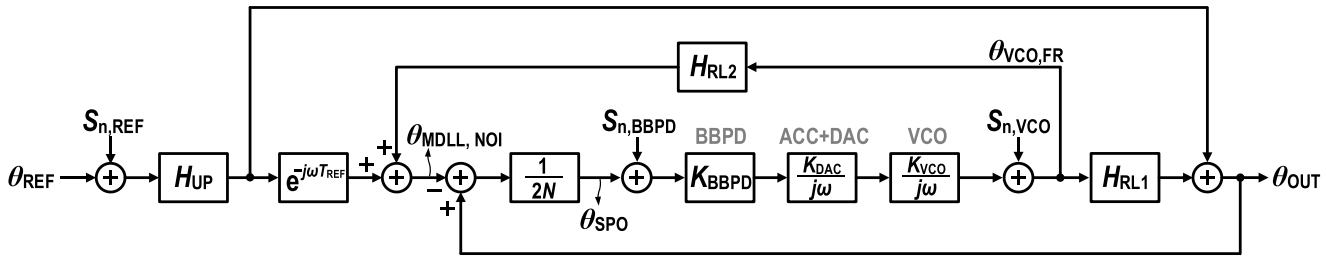


Fig. 11. Phase noise model of the proposed MDLL.

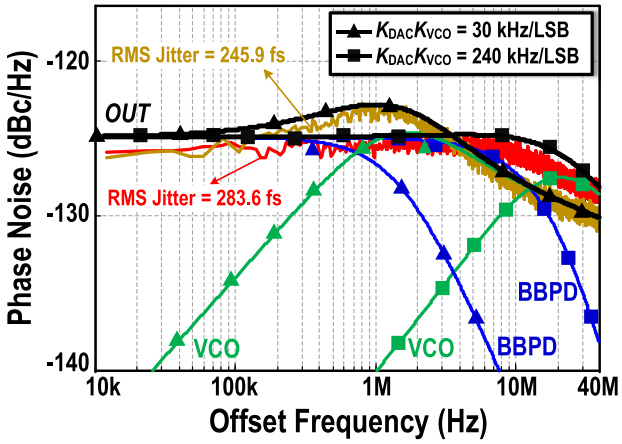


Fig. 12. Comparison between the simulated and calculated phase noise at 3 GHz ($N = 15$).

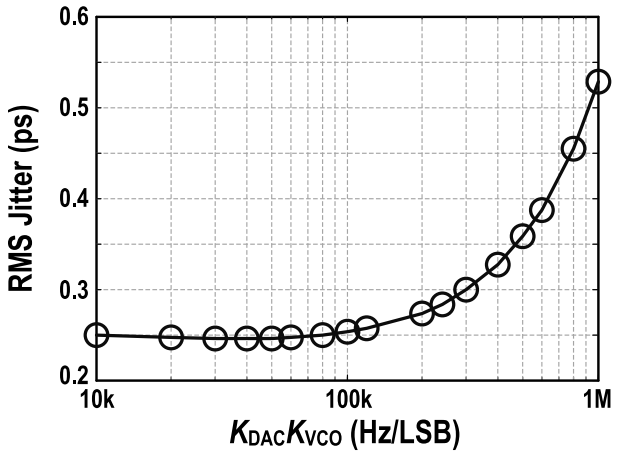


Fig. 13. Simulated rms jitter versus K_{DCO} at 3 GHz (integrated from 10-k to 100-MHz offset, excluding the REF noise and $N = 15$).

by the rms jitter of the MDLL output. In case the VCO noise dominates, the PSD of the BBPD input-referred quantization noise can be written as

$$S_{n,\mathrm{BBPD}} \approx \frac{9\pi^2}{8} \times \frac{f_{\mathrm{BW}}^2}{f_{\mathrm{BW}} \times \ln\left(1+\frac{f_{\mathrm{ref}}}{2f_{\mathrm{BW}}}\right)} \times \frac{\sigma_{\Delta t}^2}{1+\frac{f}{f_{\mathrm{BW}}}}. \quad (13)$$

The accumulator and DAC together are modeled as a continuous-time integrator $K_{\mathrm{DAC}}/j\omega$ to avoid the conversion between the continuous and discrete time domains. According to Fig. 11, the open-loop gain G_{OL} by breaking the loop at the input of BBPD and the noise transfer functions (NTFs) from the REF noise $S_{n,\mathrm{REF}}$, the VCO noise $S_{n,\mathrm{VCO}}$, and the BBPD quantization noise $S_{n,\mathrm{BBPD}}$ to the θ_{OUT} can be calculated as

$$G_{\mathrm{OL}} = K_0 \times [H_{\mathrm{RL1}} - H_{\mathrm{RL2}}] \quad (14)$$

$$\mathrm{NTF}_{\mathrm{REF}} = H_{\mathrm{UP}} \times \frac{\left(1+H_{\mathrm{RL2}}K_0 - H_{\mathrm{RL1}}K_0 \times e^{-j\omega T_{\mathrm{REF}}}\right)}{1-G_{\mathrm{OL}}} \quad (15)$$

$$\mathrm{NTF}_{\mathrm{VCO}} = \frac{H_{\mathrm{RL1}}}{1-G_{\mathrm{OL}}} \quad (16)$$

$$\mathrm{NTF}_{\mathrm{BBPD}} = \frac{2H_{\mathrm{RL1}}K_{\mathrm{o}}N}{1-G_{\mathrm{OL}}} \quad (17)$$

where K_0 is given by

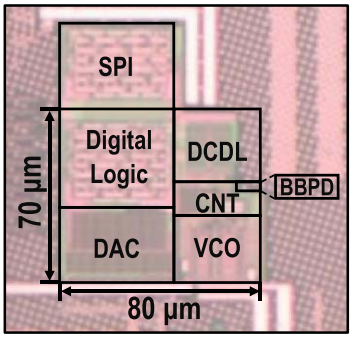
$$K_{\mathrm{o}} = \frac{K_{\mathrm{BBPD}}K_{\mathrm{DAC}}K_{\mathrm{VCO}}}{2N(j\omega)^2}. \quad (18)$$

Fig. 12 shows the comparison between the calculated output phase noise using (10)–(18) and the results from the behavioral simulation. For simplicity, we consider only the noise contribution from the VCO and BBPD, and extract $\sigma_{\Delta t}$ from the behavioral simulation to estimate K_{BBPD} and $S_{n,\mathrm{BBPD}}$ for the calculation. The free-running VCO has a phase noise of -85 dBc/Hz at 1 MHz offset and a $1/f^3$ phase noise corner of 10 MHz. The deviation between the calculation and simulation results mainly comes from the approximation of BBPD noise using (13). Since $K_{\mathrm{DAC}}K_{\mathrm{VCO}}$ directly affects G_{OL} and thus the FTL BW, a small $K_{\mathrm{BBPD}}K_{\mathrm{DAC}}$ is preferred to reduce the FTL BW, helping to suppress BBPD noise at large offset frequency (Fig. 12). As illustrated in Fig. 13, the jitter improvement will saturate when $K_{\mathrm{DAC}}K_{\mathrm{VCO}} < 100$ kHz since the increase of the VCO noise nullifies the reduction of the BBPD noise (Fig. 12). In this paper, $K_{\mathrm{BBPD}}K_{\mathrm{DAC}} \approx 240$ kHz is chosen to keep a small DAC area while still maintain a low rms jitter.

V. Measurement Results

The proposed MDLL is fabricated in 28-nm CMOS and occupies a die area of 0.0056 mm^2 as shown in Fig. 14(a). The total power consumption is ~1.45 mW at a 0.8-V supply and a 200-MHz REF clock. The detailed power breakdown is summarized in Fig. 14(b). The total power consumption is dominated by the RVCO (1.15 mW). An off-chip LDO regulator supplies the power to the RVCO.

Fig. 15 shows the measured phase noises of the open-loop VCO, the MDLL with FTL on and off at a 200-MHz REF



(a)

Power Consumption (mW)	
Digital Logic	0.2
AES and TIC*&	0.04
Counter	0.02
DAC	0.03
VCO	1.16
Total	1.45

* AES: Adjacent Channel Selector, TIC: Time-Interval Comparator.
& Power of comparison logic in AES is included in the digital logic.

(b)

Fig. 14. (a) Chip micrograph. (b) Power breakdown.

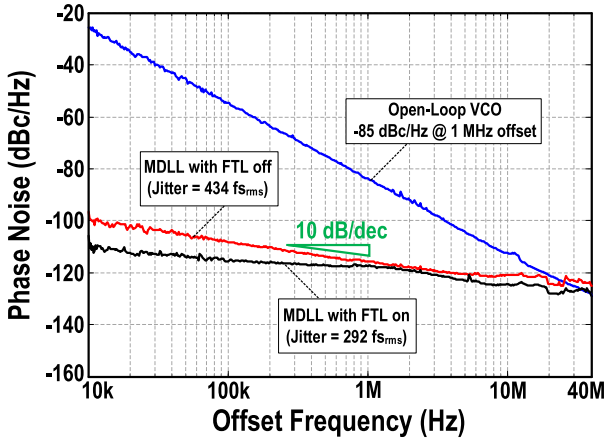


Fig. 15. Measured phase noise of the open-loop VCO and the MDLL with FTL on and off at 3 GHz.

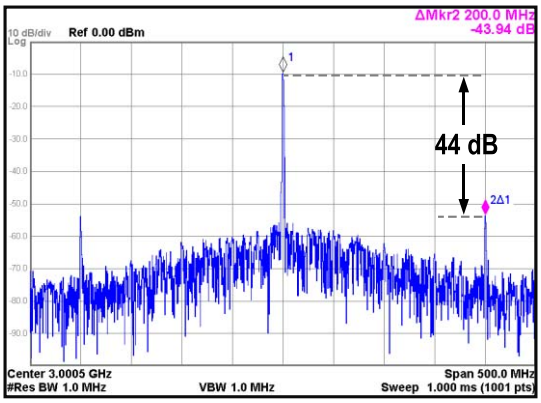


Fig. 16. Measured output spectrum of the MDLL with FTL on at 3 GHz.

clock by using the Keysight E5052B Signal Source Analyzer. When the FTL is on, the $1/f^3$ phase noise from the VCO is further suppressed and the rms jitter (integrated from 10 kHz to 40 MHz) is reduced from 430 to 292 fs which is limited by the REF noise. In practice, a low-frequency REF is preferable, which can be directly generated by a standard XO. One possible solution to generate the 200-MHz reference frequency from a standard XO is to employ an on-chip frequency doubler with a duty-cycle calibration scheme [6], [14].

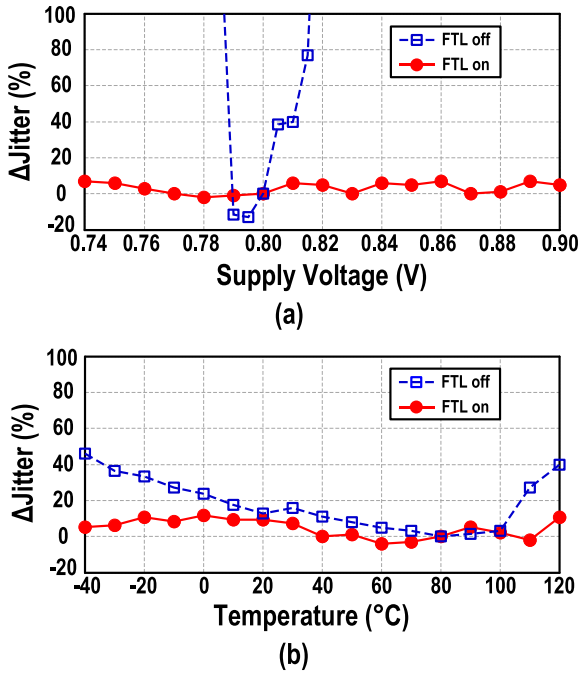


Fig. 17. Measured rms jitter versus (a) supply voltage and (b) temperature with FTL on or off.

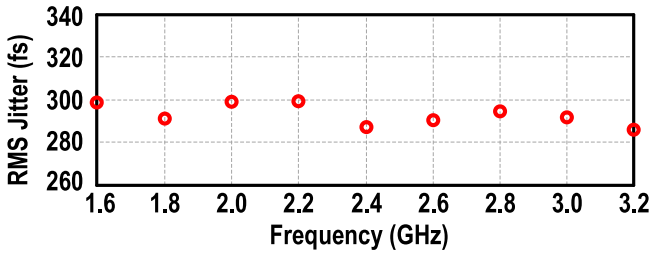


Fig. 18. Measured rms jitter versus the oscillation frequency.

Fig. 16 shows the measured spectrum of the MDLL output with FTL on at 3 GHz where the *REF* spur at 200-MHz offset is −44 dBc. The REF spur is mainly limited by the coupling from REF input to the MRVCO supplies through the bonding wire and ESD power rails which can be improved by better PAD arrangement and upsizing the REF buffer to reduce the REF input power. If we reduce the input power of the REF clock from +5 to −11 dBm, the REF spur can be improved to −52 dBc but at a cost of degraded phase noise performance due to the undersized REF buffer.

The proposed FTL can always calibrate the frequency drift of the RVCO, induced by voltage and temperature variations, as long as the desired frequency is within the frequency tuning range of the RVCO. As verified in Fig. 17(a), when the FTL is turned on, the rms jitter variation is <7% as the supply voltage changes from 0.74 to 0.9 V. When the FTL is off, the MDLL suffers from a significant rms jitter degradation even with a small supply variation. The phenomena is similar when changing the temperature as shown in Fig. 17(b).

Fig. 18 shows the measured rms jitter as a function of the output frequency, which is between 286 and 300 fs.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART RVCO-BASED MDLLS AND IL-PLLS

	This Work	[12] JSSC'17	[14] JSSC'17	[10] JSSC'13	[6] ISSCC'17	[7] ISSCC'17	[5] JSCC'16	[4] JSCC'14
CMOS Technology	28 nm	65 nm	28 nm	130 nm	65 nm	65 nm	65 nm	65 nm
Architecture	MDLL	MDLL	MDLL	MDLL	IL-PLL	IL-PLL	IL-PLL	IL-PLL
FTL Techniques	**Block-Sharing Offset-Free FTL**	Period's Error-rate Calculation	Pulse-Width Comparison	Digital FTL w/ BBPD	Pulse Gating	Symmetric PD Cancellation	Replica Delay Cell	Replica VCO
Supply (V)	0.8	1.2	1.1	1.1	0.9-1.1	1.2	1.1	1.0
Freq. Range (GHz)	1.55 – 3.35 (73.5%)	0.2-1.45 (151.5%)	2.4	0.8-2.0 (85.7%)	2.5-5.75 (78.8%)	0.52-1.15 (75.4%)	0.96-1.44 (40%)	0.5-1.6 (104.7%)
Output Freq. (GHz)	3.0	1.4	2.4	1.5	5.0	0.9	1.2	1.2
***REF* Frequency (MHz)**	200	87.5	75	375	125	150	120	300
Multiplication Ratio	15	16	32	4	40	6	10	4
***REF* Spur (dBc)**	−44	−45	−51.4	−55.6	−45	N/A	−53	−57
Integ. RMS Jitter (ps) (Integration bandwidth)	0.292 (10k-40MHz)	2.8 (10k-10MHz)	0.7 (1k-40MHz)	0.4 (10k-100MHz)	0.34 (10k-40MHz)	0.42 (10k-10MHz)	0.185 (10k-40MHz)	0.7 (10k-40MHz)
Total Power (mW)	1.45	8	1.51	0.89	5.3	3.8	9.5	0.97
FTL Power (mW)	**0.3**	3.5	0.43	0.64	2.0	2.9	4.75	0.63
FoM (dB)	**−249.1**	−225	−241.3	−248.5	−242.4	−241.7	−244.9	−243
FoM$_r$ (dB)	**−249.1**	−228.6	−245.6	−245.7	−244.4	−242.9	−247.1	−241.2
Active Area (mm^2)	**0.0056**	0.054	0.024	0.25	0.09	0.062	0.06	0.022

* $\text{FoM} = 10\log\left[\left(\frac{\sigma_{\text{rms}}}{1\text{ sec}}\right)^2 \cdot \frac{\text{P}_{\text{DC}}}{1\text{ mW}}\right]$

* Normalized to $f_{\text{REF}} = 200$ MHz, $\text{FoM}_{\text{r}} = 10\log\left[\left(\frac{\sigma_{\text{rms}}}{1\text{ sec}}\right)^2 \cdot \frac{\text{P}_{\text{DC}}}{1\text{ mW}} \cdot \frac{f_{\text{REF}}}{200\text{ MHz}}\right]$ [20]

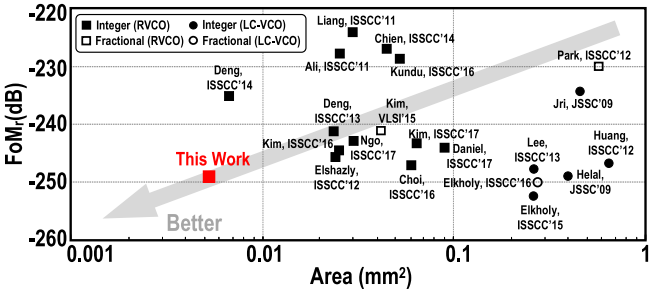


Fig. 19. Benchmark with the state-of-the-art MDLLs and IL-PLLs in terms of FoM$_r$ and area.

Table I summarizes the performance of the propose MDLL and shows the comparison of other state-of-the-art MDLLs and injection-locked PLLs (IL-PLLs). The FoM$_r$ [20] is included to count the effect of different REF clock frequencies on the jitter and power performances. This paper achieves a constant low rms jitter performance over a wide tuning of 73.5% and shows improved area efficiency ($>4.2\times$) and FoM$_r$ (>2 dB). The proposed FTL consumes the lowest power consumption of 0.3 mW. Fig. 19 also benchmarks this paper with the state-of-the-art MDLLs and IL-PLLs in terms of FoM$_r$ and area.

VI. CONCLUSION

In this paper, we presented an all-digital MDLL that features a low-power block-sharing offset-free FTL (0.3 mW) to continuously track and calibrate the SPO which guarantee a low rms jitter in the presence of PVT variations. The FTL employs an adjacent-edge selector and a DCDL-based time-interval comparator to realize a low-power SA time-length digitization and comparison scheme. The block-sharing-based SPO detection cancels the deterministic comparison error induced by the circuit mismatch and offset. The block sharing between the coarse FTL and the control generation circuits of the adjacent edge selector further reduced the FTL power consumption. The varactor-tuned dual MRVCOs help preventing the rms jitter degradation at low frequency. Thus, the MDLL achieves a low rms jitter between 286 and 300 fs over the frequency range of 1.55–3.35 GHz, with a power consumption of 1.45 mW.

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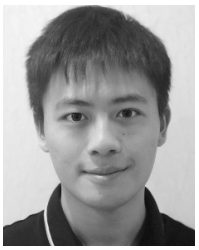

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Dr. Martins was a recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. He received the IEEE Council on Electronic Design Automation Outstanding Service Award in 2016. He was a Founding Chairman of the IEEE Macau Section from 2003 to 2005 and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications (COM) from 2005 to 2008 [2009 World Chapter of the Year of IEEE CAS Society (CASS)]. He was a General Chair of the 2008 IEEE Asia-Pacific Conference on CAS—APCCAS'2008, and was a Vice President of Region 10 (Asia, Australia, and the Pacific) of IEEE CASS from 2009 to 2011. Since then, He has been a Vice President (World) Regional Activities and Membership of the IEEE CASS from 2012 to 2013, and an Associate Editor of the IEEE TRANSACTIONS ON CAS II: EXPRESS BRIEFS from 2010 to 2013, nominated Best Associate Editor of T-CAS IIfrom 2012 to 2013. He has been a member of the IEEE CASS Fellow Evaluation Committee in 2013, 2014, and 2019, and the CAS Society representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)—the Director of the IEEE. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference—ASP-DAC'2016. He was a Nominations Committee Member of the IEEE CASS from 2016 to 2017 and the Chair of the IEEE CASS Fellow Evaluation Committee (Class 2018). In representation of UM, he was one of the Vice Presidents from 2005 to 2014 and the President from 2014 to 2017 of the Association of Portuguese Speaking Universities. In 2010, he was elected, unanimously, as Corresponding Member of the Portuguese Academy of Sciences (in Lisbon), being the only Portuguese Academician living in Asia.