Fully Integrated High Voltage Pulse Driver Using Switched-Capacitor Voltage Multiplier and Synchronous Charge Compensation in 65-nm CMOS

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***Abstract*—This brief presents a high efficiency fully integrated high-voltage (HV) pulse driver in standard CMOS. Powered by a standard I/O DC voltage of 2.5 V, the proposed system employs an optimized 4-stage cross-coupled switched-capacitor voltage multiplier (SCVM) together with an on-chip HV output driver to generate HV pulses of >10 V. We propose an area-efficient HV output driver stage to reach up to 12% total active area reduction when compared with the conventional implementation while maintaining the low static power characteristics. We also present a synchronous charge compensation (SQC) technique to alleviate the loading-dependent signal distortion through reducing the HV rail voltage droop and improving the HV pulse settling time during the driver output transitions. Fabricated in 65-nm bulk CMOS, the chip prototype can successfully generate HV pulses from 250 kHz to 1 MHz with a 15 pF load while ensuring no device breakdown. Measurement results demonstrate a peak SCVM power conversion efficiency (PCE) of 50% and an overall driving efficiency of 12.25%. The chip prototype attains a ∼2× faster output pulse transition speed compared with the state-of-the-art.**

***Index Terms*—Charge compensation, driver, fully integrated, high-voltage, square wave, switched-capacitor, voltage multiplier.**

I. Introduction

With the continuous development of micro-electro-mechanical system (MEMS)-based and piezoelectric-based devices, miniaturized capacitive sensors (e.g., gyroscopes, accelerometers, pressure sensors and resonators) are widely employed in portable consumer products, medical instruments and micro-robots [1]–[4]. Due to their small size and capacitive property, these devices typically exhibit a loading in the order of tens of pF and consume few tens to hundreds of μA [5], [6]. High driving signals in the order of few tens of volts are also necessary to ensure improved signal-to-noise ratio (SNR) and/or extended dynamic range specifications in timing and motion sensing applications [2], [3]. All these requirements mandate highly efficient integrated high-voltage (HV) signal drivers for sustaining the corresponding electrostatic actuation. Generating such a HV signal by CMOS circuits typically demands for HV devices available only in special HV fabrication processes. Yet, on-chip HV generation using standard CMOS technologies is becoming more and more attractive, with considerations of higher system performance, smaller form factor, lower cost and full system integration. Switched-capacitor voltage multiplier (SCVM) is a favorable solution due to its high power conversion efficiency (PCE) under monolithic integration [7].

Conventionally, on-chip HV generation is accomplished through cascading a SCVM stage with a HV driving stage. However, the HV output driving stage typically requires a large area overhead due to the use of special HV devices and large passives to achieve robust operation with reduced static power consumption, increasing the overall cost. To alleviate these problems, pure SCVM-based on-chip HV pulse drivers which can eliminate the HV output driving stage are proposed [8]–[9]. Fig. 1(a) illustrates the work in [9]. In the falling edge generation phase, all the flying capacitors C_B should be fully discharged to pull down the voltage on the load capacitance C_P from V_{DDH} to 0, and recharged in the rising edge generation phase. Since the capacitance of C_B can be comparable with or even greater than C_P, it can periodically induce significant energy loss and limit the achievable output driving frequency, ultimately limiting the overall driving efficiency and speed.

Tackling on the discussed limitations, this brief proposes a HV square wave driver in 65nm bulk CMOS as shown in Fig. 1(b), which employs an optimized 4-stage Dickson SCVM in a cross-coupled scheme to generate an on-chip $V_{DDH} > 10$V without extra internal DC capacitors. A low-power area-efficient HV output driver (HVOD) stage is also proposed to reduce the total area overhead by up to 12% over the conventional approach. Using the HVOD, this brief

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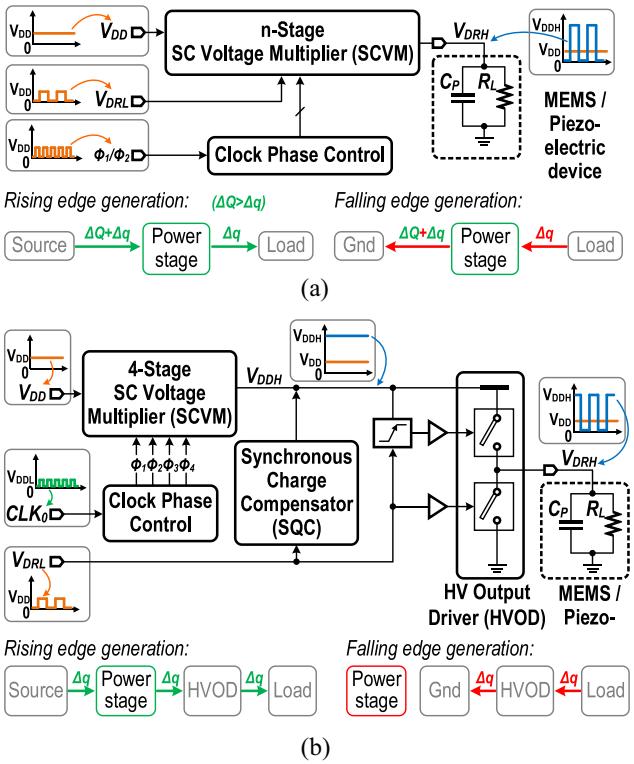

Fig. 1. Overview of (a) the existing SCVM-based [9] and (b) the proposed HV pulse driving system.

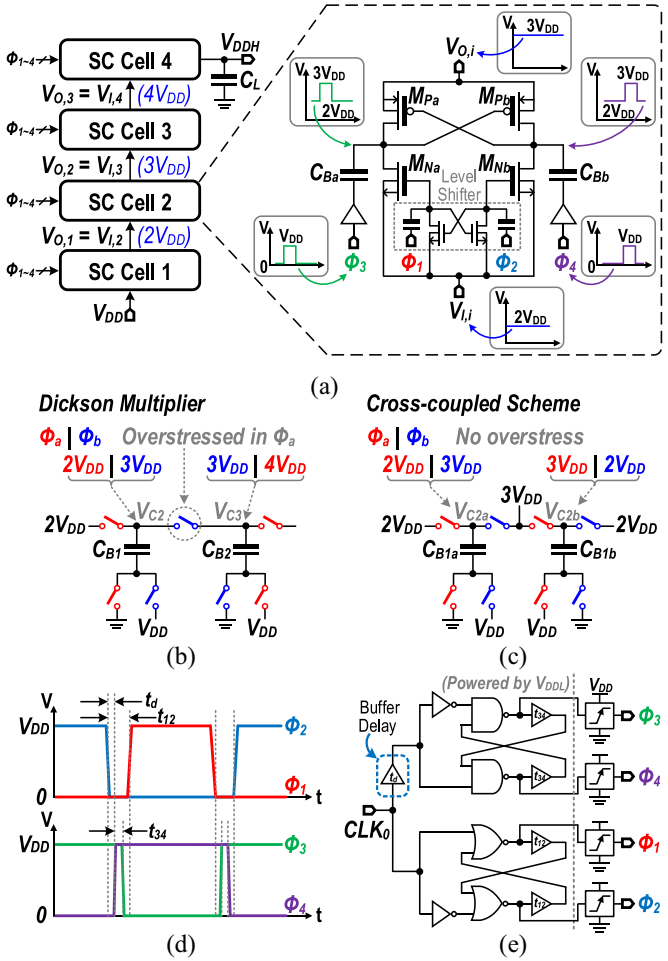

Fig. 2. (a) 4-stage SC voltage multiplier implemented by cascading the cross-coupled SCVM cells. Switch overstress demonstration of using (b) Dickson multiplier and (c) cross-coupled Dickson scheme. (d) The timing diagram of the 4-phase non-overlapping (NOV) control signals. (e) Implementation of the clock phase generator.

can avoid fully discharging/recharging of all the C_B as in [9], achieving improved driving efficiency and fast output transients. To alleviate the voltage droop in V_{DRH} during the rising edge transition due to the charge sharing between C_P and the SCVM stage, we propose a synchronous charge compensation (SQC) technique to further improve the transition speed and lower the pulse distortion.

This brief is organized as follows. Section II introduces the implementation of the SCVM stage. Section III details the design and optimization of the HV output diver circuit and the proposed SQC technique. Measurement results are shown in Section IV. Conclusions are drawn in Section V.

II. SCVM Design

Referring to Fig. 1(b), the SCVM is required to boost a standard V_{DD} of 2.5V to >10V. Accordingly, as shown in Fig. 2, a 4-stage SCVM which can theoretically provide a 5× voltage multiplication is employed. The modular SC power cells in Fig. 2(a) are implemented by using the cross-coupled scheme to generate an i-th cell output voltage of $V_{O,i} = V_{I,i} + V_{DD}$. The employed cross-coupled Dickson structure can achieve optimal conduction and bottom-plate parasitic losses, which are essential for efficient on-chip voltage conversion [10]–[11]. Moreover, the modular power cell and the relaxed voltage stress on the power switches make it attractive for HV generation using low voltage (LV) switches when compared with the other SCVM schemes, including the series-parallel, ladder, Fibonacci and exponential topologies [12].

As illustrated in Fig. 2(b), a major problem of the Dickson voltage multiplier is the necessity for the inter-cell switches to block $2V_{DD}$ during the turn-off state, which will inevitably overstress the interconnecting switches. In contrast, as can be observed in Fig. 2(c), the switches connected to the output node in a cross-coupled cell sustain only V_{DD} maximally, eliminating the breakdown risk. The cross-coupling operation ensures output charge delivery in alternate phases. The continuous output charge flow can reduce the filtering capacitor overhead at V_{DDH} with equivalent output voltage ripple requirement when compared to the conventional Dickson implementation, effectively improving the area efficiency for on-chip implementation. Furthermore, it also exhibits the inherent advantage of bootstrapping the switch driving with the power cell internal node voltages, which can save the additional switch driver design requirement. To reduce the reversion loss induced by the shoot-through current at M_{Pa} and M_{Pb} in Fig. 2(a), additional control phases are employed to introduce a dead-time $t_{NOV,34}$ between the switching cycles [13], as illustrated in Fig. 2(d). Similarly, $t_{NOV,12}$ is generated with $t_{NOV,12} > t_{NOV,34}$ to eliminate the reversion loss. To properly control the N-switches M_{Na} and M_{Nb}, a charge pump-based level shifter is adopted to adaptively boost $\Phi_{1,2}$ according to the power cell internal node condition. The implementation of a 4-phase non-overlapping (NOV) clock generator is shown in Fig. 2(e), which is designed using LV core devices and powered by the core supply voltage $V_{DDL} = 1.2$V. The generated controls are level shifted from V_{DDL} to V_{DD} (i.e., 2.5V) for proper power switch operations.

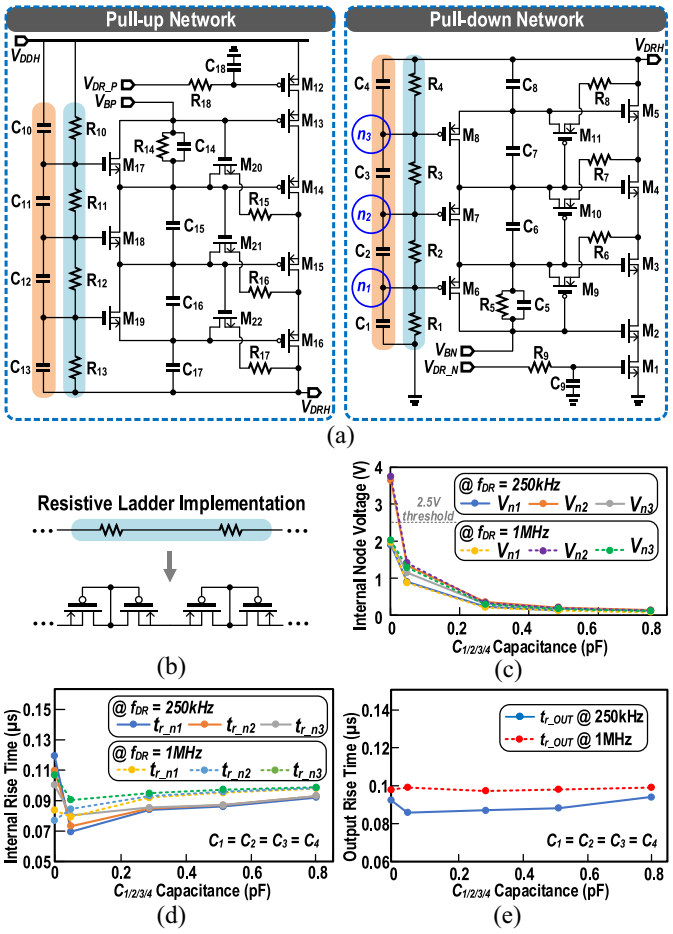

Fig. 3. Schematic of (a) the HV output driver with biasing network; and (b) the implementation of the resistive voltage divider using pseudo resistors. Simulation results showing the effect of the unit compensation capacitance to (c) the periodic steady-state internal node voltage while $V_{DRH} = 0$; (d) the internal node transition rise time t_{r_ni}; and (e) the output transition rise time t_{r_OUT}.

III. Output Driver and Charge Compensation

A. Modified HV Output Driver

To generate a high frequency HV pulse with a large capacitive load using standard I/O devices (2.5V), a stacked-transistor HV output driver [14] with biasing is designed, as shown in Fig. 3(a). The driver consists of 5 stacked P/NMOS I/O transistors ($M_{1\sim5}$ and $M_{12\sim16}$) to sustain the voltage stress from the >10V output swing. The biasing voltages V_{BN} and V_{BP} are supplied by V_{DD} and the output of the 3rd SCVM cell $V_{O,3}$, respectively. V_{DR_P} and V_{DR_N} are synchronized with the input pulse control signal V_{DRL} (from 0 to V_{DD}). The output pull-up network is controlled by V_{DR_P}, which swings from ($V_{DDH} - V_{DD}$) to V_{DDH}. Similarly, V_{DR_N} for the output pull-down control swings from 0 to V_{DD}. Consequently, the HV output driver can generate an output pulse V_{DRH} from 0 to V_{DDH}.

In practice, asynchronous change in the biasing branch can cause overstress across the stacked transistors, raising the breakdown risk. To prevent function failure due to the improper gate biasing of the stacked transistors in the driver circuit, $R_5C_5 \sim R_8C_8$ are adopted in the pull-down network. With the optimization method in [14], the output driver can guarantee well-bounded biasing conditions through proper RC selections. A similar mechanism is also applicable to the pull-up network.

Conventionally, large passive resistors $R_{1\sim4}$ and $R_{10\sim13}$ are employed in the resistive ladder as highlighted in the Fig. 3(a), and can be sized based on the available power budget. This will inevitably occupy a significant chip area. To resolve the issue, a PMOS-based pseudo-resistor ladder using small transistors (W/L = 1.5µm/440nm) with negligible parasitic capacitance is employed, as shown in Fig. 3(b). However, due to the non-linear characteristics of the pseudo-resistors, the equivalent impedance can vary according to the biasing conditions. This can affect the settling time of the internal node voltages, and the exceedingly large time constant can result in unexpected node voltages, especially when the output changes from high to low. This will in turn increase the risk of device breakdown. To compensate for this effect, we propose to connect shunt capacitors $C_{1\sim4}$ and $C_{10\sim13}$ (= 290fF) with the pseudo resistors, as shown in Fig. 3(a). The capacitive branch $C_{5\sim8}$ forms a high frequency path to pull up/down the internal node voltages during the output high/low transitions. $R_{6\sim8}$ are implemented to assist the transition of the gate biasing for $M_{3\sim5}$ during the V_{DRH} falling/rising edges. $M_{9\sim11}$ serve to connect $R_{6\sim8}$ to the gate of $M_{3\sim5}$ when V_{DRH} changes from low to high. Here, we set $R_1C_1 = R_2C_2 = R_3C_3 = R_4C_4$ to minimize the dc and ac gain difference for achieving a fast transient response, and $C_{1\sim4}$ are of the same value. Using the pull-down network as an example, Fig. 3(c) shows the schematic level simulation results for the periodic steady state voltages at $n_{1\sim3}$ of the pull-down network when V_{DRH} is low, at driving frequencies of f_{DR} = 250 kHz and 1 MHz. As observed, without the proposed capacitive path, V_{n2} can be over 2.5V which will conditionally overstress M_7. As the compensation capacitors $C_{1\sim4}$ (and $C_{10\sim13}$) increase, all the internal node voltages are properly settled to either V_{SS} or V_{DDH}. Fig. 3(d) and (e) display the effect of the unit compensation capacitance value to the rise times of the internal nodes (t_{r_n}) and the output node (t_{r_out}) of the pull-down network, respectively. In contrast to the case without $C_{1\sim4}$, the rise times of both the internal nodes and the output at 250 kHz are evidently improved with a careful selection of $C_{1\sim4}$. According to the results in Fig. 3(c)~(e), we set the capacitance of $C_{1\sim4}$ and $C_{10\sim13}$ as 0.29pF to balance between the internal node settling, transition speed and chip area. When compared with high resistivity poly resistor (~1kΩ/□) implementations, the proposed shunt capacitors together with pseudo-resistor ladder scheme can achieve a ~8× area reduction at 1 MHz operation with a power budget of ~2 µW. It corresponds to a 12% reduction in the total chip area in this brief.

B. Synchronous Charge Compensation (SQC)

Due to the charge sharing between the SCVM output capacitance C_L and the loading capacitance C_P, V_{DDH} will inevitably drop during the pull-up process of V_{DRH}, resulting in slower low-to-high edge transition. To reduce this loading dependent distortion at the HV driver output stage, the SQC technique is proposed as demonstrated in Fig. 4. The charge compensation capacitor C_{QC} cooperates with the HV output driver to deliver charge to the output, and is triggered by the same input control signal V_{DRL}. Thus, the compensation charge is injected into the V_{DDH} node synchronously at the output rising edge. Notice that both the size of C_{QC} and its bottom-plate switching voltage can affect the final voltage at V_{DDH}. In this

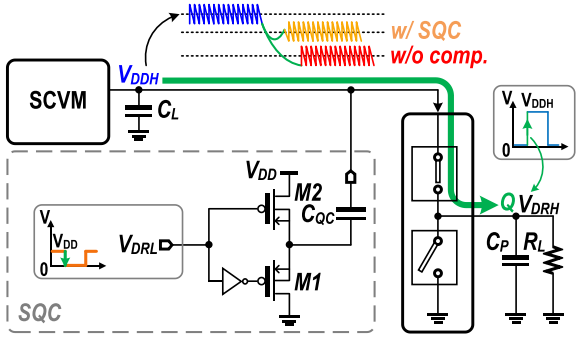

Fig. 4. The proposed synchronous charge compensation technique.

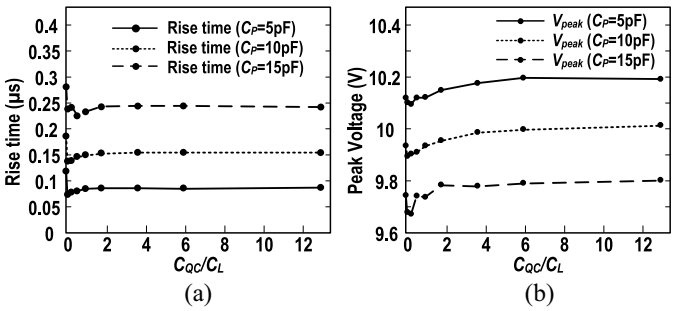

Fig. 5. Simulated effect of C_{QC}/C_L at different values of C_P on: (a) the V_{DRH} rise time; and (b) the peak achievable voltage for V_{DDH}.

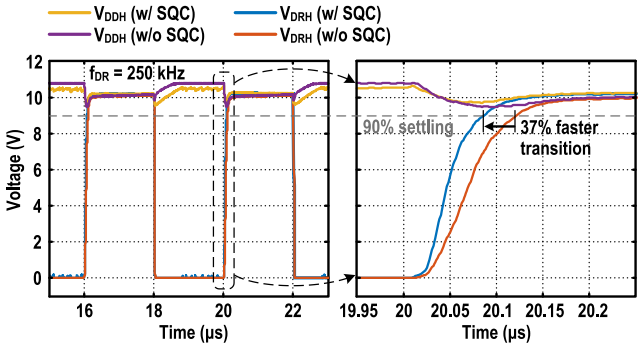

Fig. 6. Simulation results of the output transient with and without using SQC at $f_{DR} = 250$kHz.

brief, the bottom-plate of the C_{QC} is switched between V_{DD} and $\sim V_{DD}/2$ instead of $0\sim V_{DD}$ for lower bottom-plate parasitic loss. A small propagation delay is also introduced on the control path through M_1 to avoid the sudden discharge of C_L at the output falling edge, as shown in Fig. 4.

Fig. 5 displays the simulation results of the relationship between the capacitance ratio C_{QC}/C_L and the output transition time, as well as the peak achievable voltage of V_{DDH}. As observed, with a fixed total capacitance of $C_{QC} + C_L$, a $C_{QC}/C_L = 6$ is chosen to balance between the rise time and chip area. Fig. 6 shows the simulated output transient response with and without using the proposed SQC technique. It can be observed that the 90% transition time at the rising edge can be reduced by ~37% with the SQC. The proposed HVOD circuit is also robust against PVT variations based on simulation.

IV. Chip Implementation and Measurement

The proposed HV pulse driver was implemented in 65-nm bulk CMOS using 1.2-V/2.5-V transistors. The SCVM employs metal-insulator-metal (MIM) capacitors with each $C_B = 0.8$pF. The total capacitance of C_{QC} and C_L is 70pF with $C_{QC}/C_L = 6$. Fig. 7 shows the annotated chip micrograph, occupying an active area of 0.265mm^2. The SCVM together with C_L takes up ~0.1mm^2.

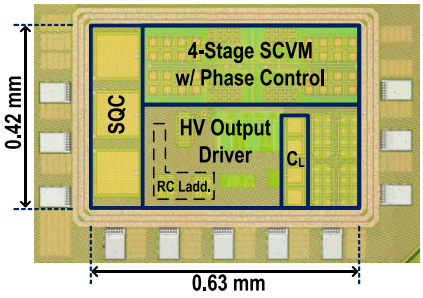

Fig. 7. Annotated chip micrograph.

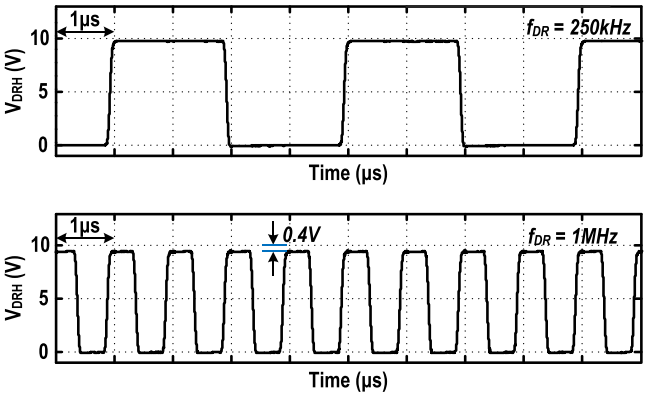

Fig. 8. Measured transient waveforms of the HV square wave output at 250 kHz (top) and 1 MHz (bottom).

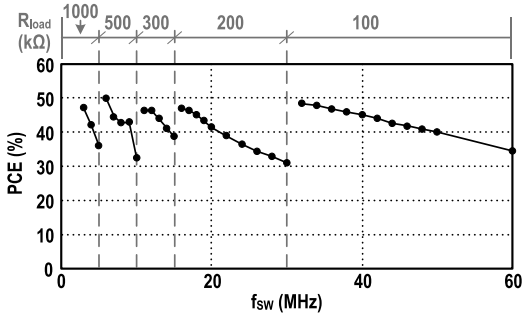

Fig. 9. Measured PCE of the SCVM over a wide switching frequency range with a loading from 100 kΩ to 1 MΩ and $V_{DDH} > 10$V.

Fig. 8 displays the measured output HV waveform at 250 kHz and 1 MHz with $V_{DD} = 2.5$V. Clocked at $f_{SW} = 32$ MHz, the on-chip SCVM generates a HV DC voltage of $\sim 4V_{DD}$ while driving a 250 kHz HV output pulses. A slight degradation at V_{DDH} of ~4% can be observed as the output driving frequency increases to 1MHz. Fig. 9 shows the measured peak PCE of the SCVM with different loading from 100 kΩ to 1 MΩ, with f_{SW} varied accordingly from 1 MHz to 60MHz to support the change in the loading condition. The measured maximum peak PCE is up to 50%.

Fig. 10 shows the measured equivalent SCVM output impedance (R_{OUT}) with a 100 kΩ loading, demonstrating high consistency with the simulation results. The no load power consumption increases due to the excessive switching loss as

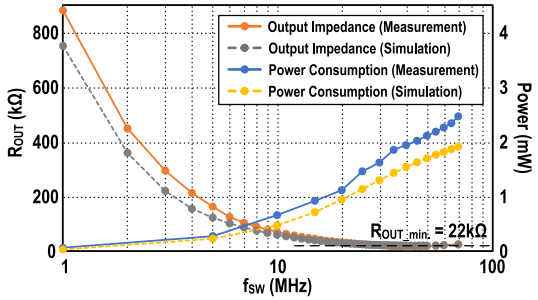

Fig. 10. Measured equivalent output impedance with a 100 kΩ loading, and the no load power dissipation of the SCVM with different f_{SW}.

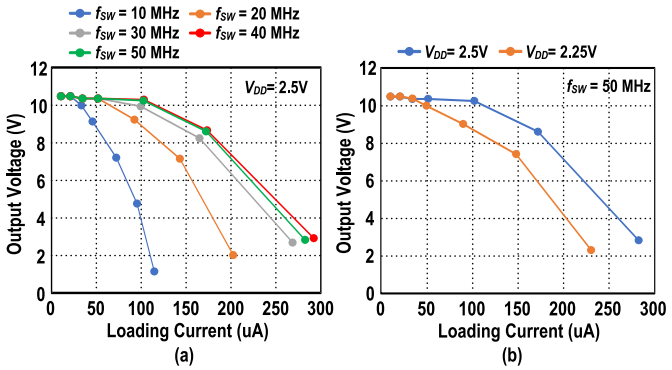

Fig. 11. Measured SCVM V-I characteristic with (a) different f_{SW} at V_{DD} = 2.5V, and (b) different V_{DD} at fixed f_{SW} = 50MHz.

TABLE I
PERFORMANCE SUMMARY AND BENCHMARK

	JSSC'16 [4]	ASSCC'14 [9]	ISSCC'14 [15]	**This work**
CMOS Tech. (nm)	130	65	65	**65**
SCVM Stage no.	3	5	17	**4**
V_{DD} (V)	3.3	2.75	2.75	**2.5**
SCVM Output (V)	10	12	34	**10**
Core Area (mm^2)	2.19	0.056	0.152	**0.265**
Pulsed Output	Yes	Yes	No	**Yes**
Capacitive Load	5nF	67pF	N/A	**15pF**
SCVM Peak Effi.	80%	63.5%	38%	**50%**
$I_{OUT,MAX}$ @ $V_{OUT,target}$	93μA	80μA	10μA	**100μA**
SCVM Power Density (mW/mm^2)	*0.015 @ 80% PCE	*15.7 @ 59% PCE	*4.1 @ 38% PCE	**10.1 @ 49% PCE**
# Driving Efficiency @ 250kHz	*4.35%	*4.7%	N/A	**12.25%**
Rise/Fall Time (ns)	513/513	330/330	N/A	**166/111**

* Estimated from the reported data. # Driving Efficiency = $\left(\frac{V_{peak}^2}{2R_{load}}\right)/P_{IN}$.

f_{SW} increases. Fig. 11 depicts the measured V-I characteristic of the SCVM operated at different f_{SW} with V_{DD} at 2.5V. With f_{SW} > 30 MHz, the SCVM can generate a stable output >10V while delivering a maximum current of 100μA. As V_{DD} reduces by 10%, i.e., from 2.5 to 2.25V, the SCVM can still deliver a loading of 50μA at output >10V. With the SCVM operating at f_{SW} = 42 MHz, the measured SCVM end-to-end driving efficiency can be up to 12.25% when generating a output pulse at 250kHz with a loading of 15pF//50 kΩ.

The measured performances for the proposed HV pulse driver are summarized in Table I, together with the comparisons with the state of the art. When compared with [9], this brief achieves an estimated 260% improvement to the overall driving efficiency while attaining a ∼2× faster output pulse rising-edge-transition speed. We have tested a total of 10 chip samples without any breakdown issue.

V. CONCLUSION

This brief presented the design and implementation of a fully integrated HV pulse driver in standard 65-nm bulk CMOS, capable of generating an output pulse amplitude of over 10V using 2.5-V devices without any breakdown issues. We designed an optimized 4-stage SCVM with reduced reversion loss to generate an on-chip HV driving rail. The output driver stage attains a 12% total area reduction through the optimization of the stacked-transistor biasing network without overstressing the devices. The proposed synchronous charge compensation technique can also effectively reduce the loading dependent voltage droop at the SCVM output. Compared with the state-of-the-art, the output transition speed is ∼2× faster.

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