Design and Control of An Integrated 3-Level Boost Converter under DCM Operation

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***Abstract*—A 3-level boost (3LB) converter has the characteristics of higher voltage conversion efficiency, lower inductor current ripples, output voltage ripples and voltage stresses on switches when compared with the conventional boost converters in continuous conduction mode (CCM). When the 3LB is integrated on a chip, we cannot avoid its discontinuous conduction mode (DCM) operation due to a small inductance and load variation. In this paper we'll present and discuss the design and control of a 3LB converter in DCM operation, implemented in a 65-nm CMOS process. Transistor level simulation results show that it operates at 100 MHz with a 5nH inductor, a 4nF output capacitor and a 2.5nF fly capacitor achieving an output conversion range of 1.5V to 2.1V from a 1.2 V input supply, with a peak efficiency of 83.2%@90mW, a load transient response of 141mV and 1.64ns/mA for undershoot, 136mV and 1.93ns/mA for overshoot, and a voltage ripple less than 60/85mV when I_{Load}=40/80mA with a typical and the maximum output voltage ripple of less than 90mV in the worst corner.**

Keywords—3-level boost converter; DCM; fast transient response; low ripple; voltage mode controller

I. INTRODUCTION

Many portable products as MPEG-3 players, personal digital assistants, wearable devices, portable medical diagnostic equipment, and internet-of-things (IoT), call for voltage boosting DC-DC converters. For such applications, the output voltage ripple, conversion ratio, and noise must be considered. For the conventional boost converters, their output currents pulsate, thus leading to large output voltage ripples. A 3-level boost (3LB) converter for continuous conduction mode (CCM) operation has been proposed in [1-3] to reduce inductor current ripples, output voltage ripples and voltage stresses on switches, thus yielding a higher conversion efficiency than the boost converter. Both 3LB and boost converters have the same CCM voltage gain and small signal transfer function for the closed-loop controller design. When a 3LB converter is designed in an integrated circuit, due to a smaller inductance and load variation, its discontinuous conduction mode (DCM) operation, cannot be avoided for longer battery life [4]. The DCM operation analysis of the 3LB converter, which includes CCM/DCM operation boundary, DCM voltage gain, and DCM small signal transfer function has been studied and proposed in a previous work [4].

Among the existing literatures, the design and control of the DCM closed-loop controller of a 3LB converter will be initially proposed and discussed in this paper, including the required gate voltages for driving the power MOSFETs of the 3LB converter, in which the proposed closed-loop controller and gate voltage signals are the main contributions of this paper. The 3LB converter is finally designed based on a 65-nm CMOS process. And its initial start-up control is not included in this paper.

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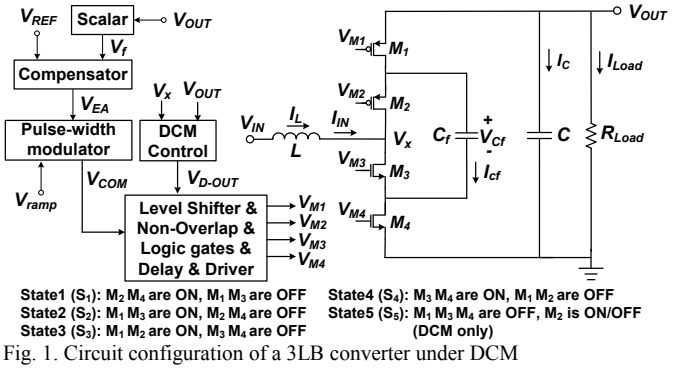

Fig. 1. Circuit configuration of a 3LB converter under DCM

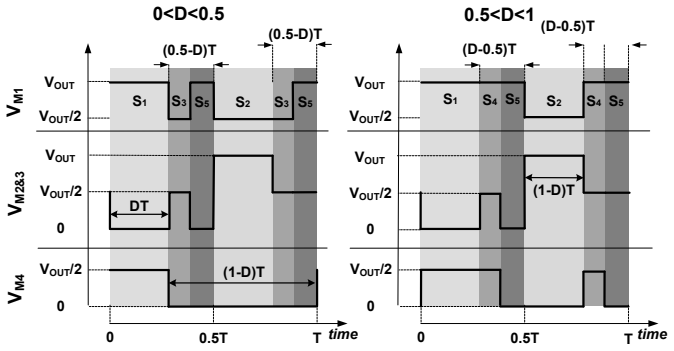

Fig. 2. Gate voltages for $M_{1\text{-}4}$ when 0<D<0.5 and 0.5<D<1

Fig. 1 shows the circuit configuration of the 3LB converter under DCM, in which V_{IN}, V_{OUT} and V_{REF} are the DC input, output and reference voltages; C_f and V_{Cf} are the flying capacitor and its voltage ($V_{Cf} = 0.5V_{OUT}$); L and C are the inductor and capacitor; R_{load} is the load resistor; I_{IN}, I_{Load}, I_{cf}, I_L and I_C are the input, load, flying capacitor, inductor and capacitor currents; $S_{1\text{-}5}$ are the different operation states; $M_{1\text{-}4}$ are the power transistor switches. A compensator is used to obtain a stable and fast control loop. A pulse-width modulator (PWM) generates the control signal V_{COM}, then this control signal is sent to the level shifter, logic gates, delay, non-overlap and driver circuits to generate the final trigger signals $V_{M1\text{-}4}$ for the $M_{1\text{-}4}$ in Fig. 2 and we use the DCM control to trigger S_5. Fig. 3 shows the 3LB converter inductor voltage V_L and current I_L waveforms for DCM when 0<D<0.5 and 0.5<*D*<1, where *D* is the duty ratio. For CCM, S_5 does not exist.

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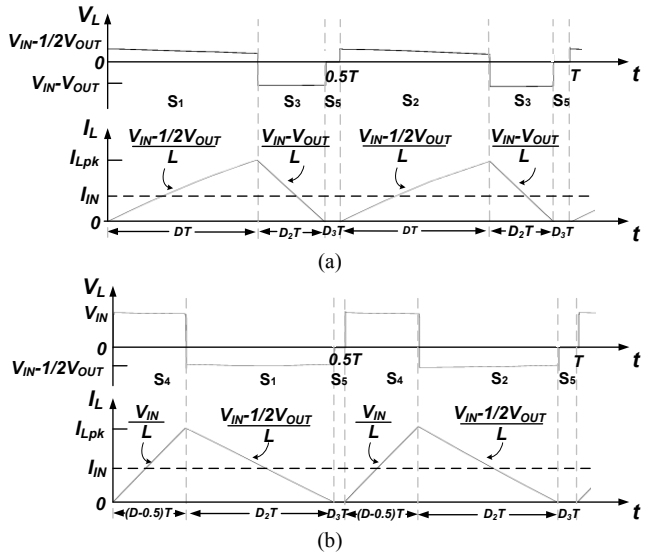

Fig. 3. 3LB converter V_L and I_L waveforms for DCM: (a) when 0 < D < 0.5, and (b) when 0.5 < D < 1

Based on the deduced DCM model in [4] and with the help of [5], a 100MHz operation frequency, a 1.2V voltage supply (V_{IN} & V_{DD}) 3LB converter will be designed for providing 1.5-2.1V (target 1.8V) output voltage (V_{OUT}), and 5-80mA load current (I_{Load}). In Section II, the design of the voltage mode controller with a compensator circuit for the 3LB converter will be presented, which consists of a ramp generator, an error amplifier (EA), a comparator and a DCM control. In Section III, transistor level simulation results will be presented, and the comparison with the state-of-the-art inductive based boost converter will also be discussed. Finally, we draw the conclusions in Section IV.

II. Design of DCM Closed-Loop Voltage Mode Controller for 3-Level Boost Converter

A. Voltage Mode Controller

A voltage mode controller, which adjusts the duty cycle in response to the output voltage changes, has the advantages of design simplicity with only one loop, low power consumption, and good noise margin for a stable modulation process [5]. Fig. 4 shows the DCM voltage mode controller for a 3LB converter.

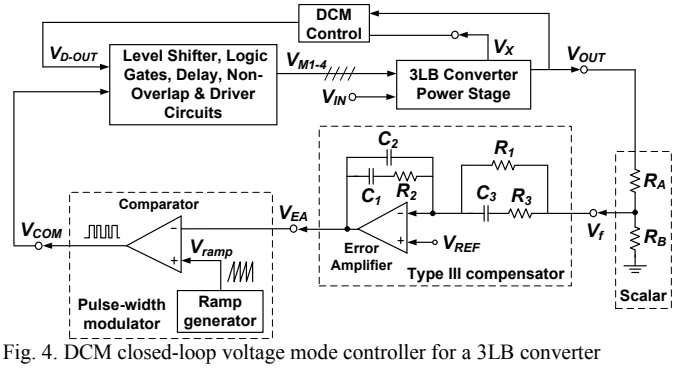

Fig. 4. DCM closed-loop voltage mode controller for a 3LB converter

The output feedback voltage V_f ($1/3V_{OUT}$) from the scalar (R_A=2R_B=20kohms) will be firstly compared with the reference voltage V_{REF} through a compensator. Then the error amplifier (EA) output voltage V_{EA} will compare with a fixed frequency ramp voltage V_{ramp}, then the output control signal V_{COM} from the comparator will be sent to the level shifter, logic gates, delay, non-overlap and driver circuits to generate the control signals for the power transistor switches ($M_{1\text{-}4}$) in the 3LB converter. The DCM control will be triggered when the reverse current is detected by comparing the output voltage V_{OUT} with V_x. When the DCM control is activated, this will adjust the control signals $V_{M1\text{-}4}$ for $M_{1\text{-}4}$. Finally, the function of the closed-loop voltage mode controller ensures a stable V_{OUT}=3V_{ref}.

B. Type III Compensator Design

The 3LB converter exhibits a right hand plane zero similar to the conventional boost converter, thus it is important to improve the stability of the 3LB converter by just using a compensator. A Type III compensator can theoretically boost the phase up to +180° at the crossover frequency, and therefore it can provide the required phase boost to maintain the overall 3LB converter at a reasonable phase margin (PM) in CCM. On the other hand, with appropriate design of the system parameters, Type II compensator already works fine for the 3LB converter under DCM operation. However, if both CCM and DCM operational modes are considered for the 3LB converter, Type III compensator should be applied to guarantee the system stability. Fig. 4 shows the circuit diagram of the Type III compensator, which comprises an error amplifier, 3 resistors and 3 capacitors [5]. After apprehending the structure of the Type III compensator network (Fig. 4) it can be mentioned that the DCM gain and gain margin (GM), as well as the PM at the crossover frequency (20MHz, 1/5 of operation frequency as usual) [4], a Type III compensator with $R_1/R_2/R_3$=25/35/2.5kΩ and $C_1/C_2/C_3$=425/ 160/555fF, already ensures a sufficient PM of 60°, as Fig. 5 shows, to obtain a stable controlled output voltage V_{OUT}.

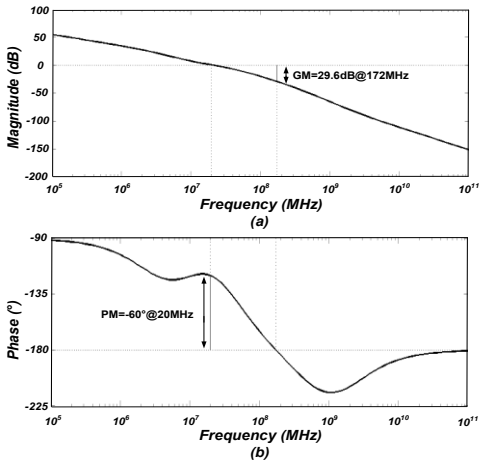

Fig. 5. A 3LB converter with Type III compensator: (a) magnitude plot and (b) phase plot at different frequencies

C. Single Boundary Ramp Generator

When the switching frequency is high (e.g. ≥100MHz), the delay in the comparator will introduce error in the ramp signal magnitude and frequency of the conventional double-boundary ramp generator. Thus, to relax this delay problem we utilized in the paper a single boundary ramp generator, proposed before in [6] (Fig. 6). With V_H=0.4V, after being controlled by the level shifter, a 100MHz (10ns period) and 0.4-0.8V ($1/2V_{DD}\pm0.2V$) voltage boundary range of the ramp signal V_{ramp} has been built, with a power consumption of 0.182mW.

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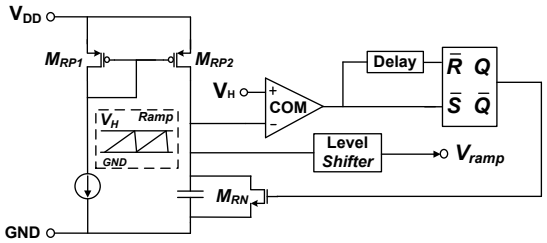

Fig. 6. Single boundary ramp generator

D. Error Amplifier (EA)

A cascade error amplifier (EA) architecture, as shown in Fig. 7, has been chosen for the high gain and speed, low power consumption and low noise EA design. In the parameter analysis, the output voltage of the EA (V_{EA}) cannot reach the V_{ramp} boundary range until the gain >27dB and GBW >46MHz. After tuning, we got a 0.212mW power consumption with 42.3dB gain and 82.9MHz GBW EA performance, which fits well in the 40 times Monte Carlo simulation.

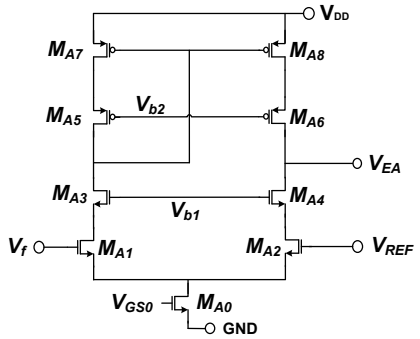

Fig. 7. Error amplifier

E. Comparator

In this design, we need a comparator for the PWM, ramp generator circuit and DCM control. Then, Fig. 8 shows a two-stage comparator circuit topology implemented by a source-coupled differential pair with positive feedback to provide a high gain [7] for the PWM and ramp generator parts. In the parameter analysis, the offset of the comparator does not affect the output side much due to the feedback network, and the power consumption of the comparator is 0.198mW.

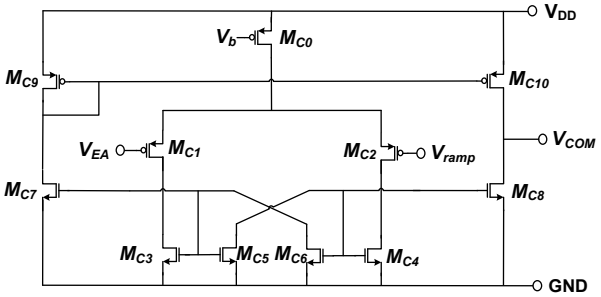

Fig. 8. Two stage comparator

F. DCM Control (ZCD)

The DCM control (ZCD) circuit first compares the signals V_{OUT} with V_x, when $V_{OUT} > V_x$, meaning that a reverse current happens, and the operation state S_5 is triggered to turn off all the power transistor switches. The DCM control circuit of Fig. 9 has been designed to withstand a high voltage and aims to reduce the reverse current during DCM by the offset designed on $M_{DP1\&2}$, also shown in Fig. 9, to maximize the efficiency of the 3LB converter [8]. Fig. 10 shows that the DCM control can reduce the reverse current problem and it exhibits a power consumption of 0.342mW. From Fig. 10, the residual reverse current is due to the delay of the control path, which is mainly contributed by the comparator and drivers. To overcome the delay problem, the idea of the DCM calibration control loop proposed in [6] can be further investigated for the 3LB converter in future work.

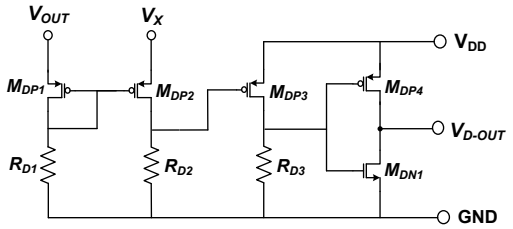

Fig. 9. DCM control

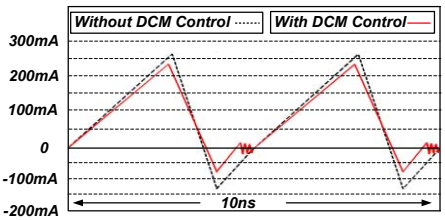

Fig. 10. Inductor current comparison without/with DCM control

III. Simulation Results

The 3LB converter is built at transistor level with 65nm CMOS parameters, from a set of designed elements: V_{IN}=V_{DD}=1.2V, L=5nH with 50mΩ, C_f=2.5nF with 75mΩ, C=4nF with 120 mΩ, R_{Load}=22.5Ω-360Ω. After constructing the 3LB converter in Cadence, the typical, corner and Monte Carlo simulation results of V_{OUT} and I_{Load}, power efficiency, output voltage ripple $V_{OUT\text{-}Ripple}$, load transient response will be provided next.

A. Typical (TT) Simulation Results

Fig. 11(a) shows the TT simulation results of V_{OUT} swings from 1.5V to 2.1V when I_{Load}=80mA, while Fig. 11(b) shows the TT simulation results of I_{Load} swings from 5mA to 80mA when V_{OUT}=1.8V. When the 3LB converter is operating in DCM with I_{Load}=5-80mA and V_{OUT}=1.8V, the active closed-loop controller consumes a constant power of 0.9mW.

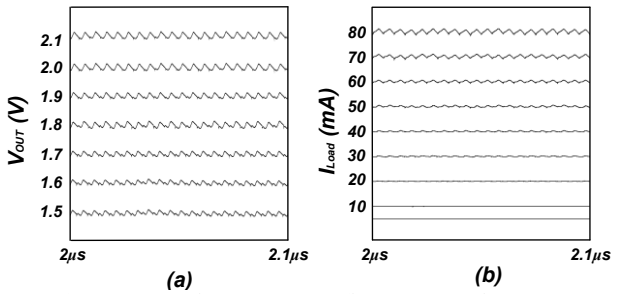

Fig. 11. (a) V_{OUT} range when I_{Load}=80mA, (b) I_{Load} range when V_{OUT}=1.8V

B. Corner Simulation Results

To ensure the performances of the 3LB converter even under process variation, different corner situations are also simulated and presented here besides the typical case.

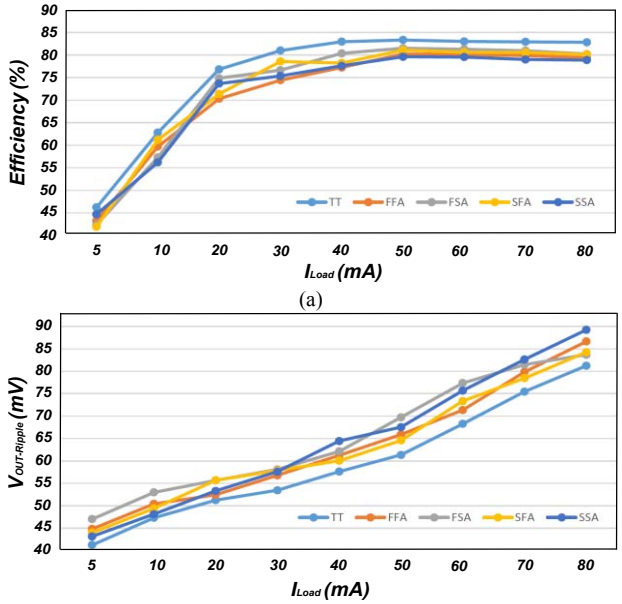

Fig. 12. 3LB converter efficiency and $V_{OUT\text{-}Ripple}$ verus I_{Load} (I_{Load}=5-80mA) when V_{OUT}=1.8V: (a) Efficiency and (b) $V_{OUT\text{-}Ripple}$ under different corners

Fig. 12 shows the trend of the conversion efficiency and $V_{OUT\text{-}Ripple}$ of the 3LB converter when I_{Load} is increasing from 5mA to 80mA under different corners. The maximum power efficiency reaches 83.2% when I_{Load}=50mA in the typical case, and the $V_{OUT\text{-}Ripple}$ at the maximum power efficiency point is smaller than 65mV. With the I_{Load} changing from 80mA to 5mA, and then back to 80mA again, the load transient response waveforms of the 3LB converter at different corners are shown in Fig.13, with the worst corner results of 148/152mV for under/overshoot voltages and with 205/184ns of settling time.

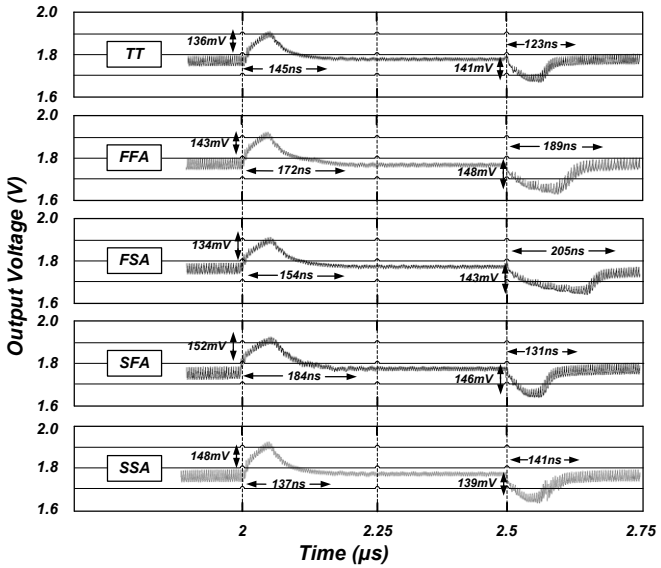

Fig. 13. Tranisent response time when I_{Load} changes from 80mA to 5mA, then back to 80mA with V_{OUT}=1.8V

C. Monte Carlo Simulation Results

Fig. 14 shows the Monte Carlo simulation results of V_{out}, Efficiency and $V_{OUT\text{-}Ripple}$. From 40 times Monte Carlo simulation results (Fig. 14) with mismatch considerations, V_{OUT} fluctuates from 1.77V to 1.84V, with an average value of V_{OUT}=1.81V, which means that the influence of EA and comparator offset are acceptable. And the Efficiency fluctuates from 77% to 85%, with an average value of 81.6%. On the other hand, the $V_{OUT\text{-}Ripple}$ fluctuates from 60mV to 100mV, with an average value of 76mV.

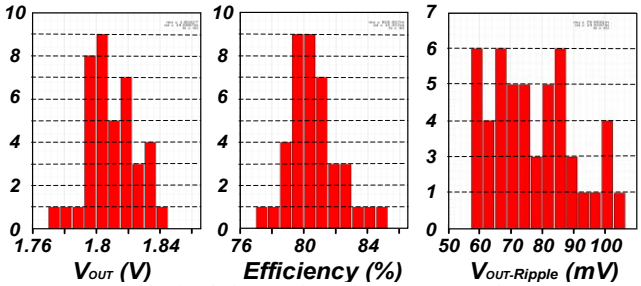

Fig. 14. Monte Carlo simulation results with V_{OUT}=1.8V and I_{Load}=80mA

D. Comparison with the-State-of-the-Art Boost Converters

When compared with similar switching frequency converters from [9] and [12], the 3LB converter can obtain higher peak efficiency and efficiency @10mA and better load transient performances. If we consider a comparison with the works from [10] and [11], the 3LB converter requires much smaller passive components (L and C) and obtains similar peak efficiency and load transient performances. Finally, if compared with all converters from [9] to [12], the 3LB converter can obtain the fastest settling time per load transient.

TABLE I. COMPARISON WITH THE-STATE-OF-THE-ART BOOST CONVERTERS [9] – [12]

	D. Bhatia JSSC 2013 [9]	Z. Sun TCAS-II 2014 [10]	Y.-S. Hwang IEEE Sens. J. 2016 [11]	S. Dam TPEL 2018 [12]	This work (TT)
Topology	Inductive Boost	Inductive Boost	Inductive Boost	Inductive Boost+LC	3-Level Boost
Process /nm	130	65	180	180	65
Frequency /MHz	100	1	1-2	118	100
Inductor (L) /nH	22*4	22000	3300	20	5
Capacitor (C) /nF [(C_f)/nF]	20	5000	10000	1.08	4 [2.5]
Input voltage (V_{IN}) /V	1.2-2	0.42-0.6	0.8-1.2	1-2.7	1.2
Output voltage (V_{OUT}) /V	3-5	0.6-0.9	1.8	3.2	1.5-2.1
Load current (I_{Load}) /mA	10-84	10-110	5-100	6-65	5-80
Load transient step (ΔI_{Load}) /mA	40	30-60	10-100	6-40	5-80
Peak Efficiency /% (@mW)	64@180	86@99	90@36	77.4@103	83.2@90
Efficiency@10mA /%	48	55	82	63	63.2
V_{OUT} under/overshoot (mV)	170/220	50/-	50/65	192/130	141/136
Settling time under/over (ns)	800/1070	100000	6000/4000	650/650	123/145
Settling time per ΔI_{Load} under/over (ns/mA)	20/26.8	3333.3/-	66.7/44.4	19.1/19.1	1.64/1.93
Max. $V_{OUT\text{-}Ripple}$ /mV	200	>100	45	21	<85

IV. CONCLUSIONS

A 1.2V voltage supply 100MHz integrated voltage mode controlled 3LB converter has been designed in 65 nm CMOS. It can achieve 1.5-2.1V output voltage and 5-80mA load current. Simulation results show that the 3LB achieves a peak efficiency of 83.2%@90mW, load transient response of 141mV and 1.64ns/mA for undershoot, 136mV and 1.93ns/mA for overshoot, and voltage ripple less than 60/85mV when I_{Load}=40/80mA in a typical case with a maximum output voltage ripple of less than 90mV in the worst corner, similar to the state-of-the-art.

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